FREQUENCY DOMAIN AND TIME DOMAIN CASCADED CIRCUIT ANALYSES USING A HEWLETT-PACKARD PROGRAMMABLE CALCULATOR

by

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Frequency Domain and Time Domain Cascaded Circuit Analyses using a Hewlett-Packard Programmable Calculator

By C.H.C. LI

ABSTRACT

This dissertation deals with a numerical technique to analyse cascaded circuits using a programmable calculator. Programs to achieve the frequency domain and the time domain circuit analysis capabilities are developed.

In the frequency domain analysis, the program accepts a wide variety of circuit components including R-L-C lumped circuit elements, transmission line type of circuit components, impedance inverters and ideal transformers. A transistor, connected in cascade, is also acceptable via a simple hybrid π model employing a voltage controlled current source to represent the active circuit element. Furthermore, for microwave circuit analysis applications, a circuit block, characterized by scattering parameters, is also provided. Equipped with swept frequency analysis capability, this program is able to compute the system performance as a function of frequency.

In the time domain circuit analysis, the program accepts R-L-C lumped circuit elements and performs analysis on the initially relexed circuit. The output time function is numerically calculated for a given input excitation.

While the principle of circuit analysis and the programming techniques described in this dissertation is applicable to any computer (programmable calculator) system, the programs are developed specifically for a Hewlett-Packard programmable calculator, model 9100B, linked to an extended memory unit, model 9101A. The computed results are presented by the accompanying printer and the X-Y plotter.

CHAPTER 1

INTRODUCTION

1.1 General

With the present day advances of computer aided design techniques [1], it is a common practice to analyse a moderately sized circuit by a computer. While most of the computer programs are capable of analysing a very complex circuit of an extremely general topology, very often, the circuit under consideration can be described by a simple topology, therefore requiring a very small portion of the total program analysis flexibility. It is felt that with the development of special circuit type analysis programs, the capability of a computer with a given memory size can be extended.

The cascaded circuit type, in particular, is of special importance to the analogue circuit designers dealing with circuits from radio frequency to the microwave frequency range. In this frequency area, most of the circuits, for example: filters and amplifiers, can be described adequately by cascades of ladder networks. It is the purpose of this dissertation to deal specifically with this class of circuits.

A Hewlett-Packard programmable calculator system is chosen as the computing tool in this investigation. It is worth noting that using this approach of 'Special circuit Type Programming' instead of the attempt to solve a general circuit [2], the analysis capability of the program is extended to be able to analyse over 18 cascaded circuit blocks of mixed lumped and distributed parameter elements in the frequency domain, and a maximum of 9 independent energy storage elements in the time domain, despite its rather limited memory size.

The obvious advantage of using a programmable calculator for circuit analysis is the possibility of a very close interaction between the machine and the operator. Any programming alteration and error correction can be made instantly and the operational cost is very small compared to operating a time-shared computer terminal.

1.2 Scope of the Dissertation

This dissertation describes the development of the circuit analysis programs for the cascaded networks using a Hewlett-Packard programmable calculator model 9100B equipped with the extended mrmory unit, model 9101A. Due to the limited

memory size of the calculator, the frequency domain and the time domain circuit analyses are performed separately by two independent program systems.

Both circuit analysis programs have their individual input sub-programs, circuit analysis sub-programs, and output sub-programs. In the frequency domain analysis, sub-routines are prepared for calculating circuit functions such as input impedance, output impedance, and the transfer function. For microwave circuit analysis applications, the output function also include reflection coefficients, voltage standing wave ratio, insertion transmission, and impedance plot on Smith Chart. The program can also accept Scattering Parameter characterization of describing a circuit block (e.g. a transistor). In the time domain circuit analysis, the desired circuit function in the complex frequency domain ($S = \sigma + j\omega$) is first formed as the ratio of two polynomial functions of 'S'. A differential equation is then formed, which is to be solved by finite difference technique. The programs developed to solve the difference equation will compute numerically the output time function for a given input excitation.

In Chapter 2, cascaded circuit analysis technique is discussed, leading to the formation of the theoretical basis for the two programs. Also included is a general description of the frequency and time domain analysis

programs to highlight the special features in both systems.

Detailed discussion of both programs are presented in Chapter 3 and Chapter 4 respectively. To further clarify the correct operation of the programs, users' guides are also given and supplemented by examples.

Chapter 5 contains the conclusion based on the performances of the programs. Comments and possibilities of any further improvements in the programs are also discussed.

For completeness, the programming steps of the individual sub-programs are presented in Appendix I and Appendix II. The programs are presently being stored on the magnetic cards from Hewlett-Packard and can be duplicated.

1.3 The Hewlett-Packard Programmable Calculator System

To present a global picture of the calculator system used in this dissertation, a brief discussion of the overall system is given here. It is assumed that the user of the analysis programs has a general understanding of the Hewlett-Packard desk-top programmable claculator programming procedures.

Presented in Fig. 1.1 is the block diagram of

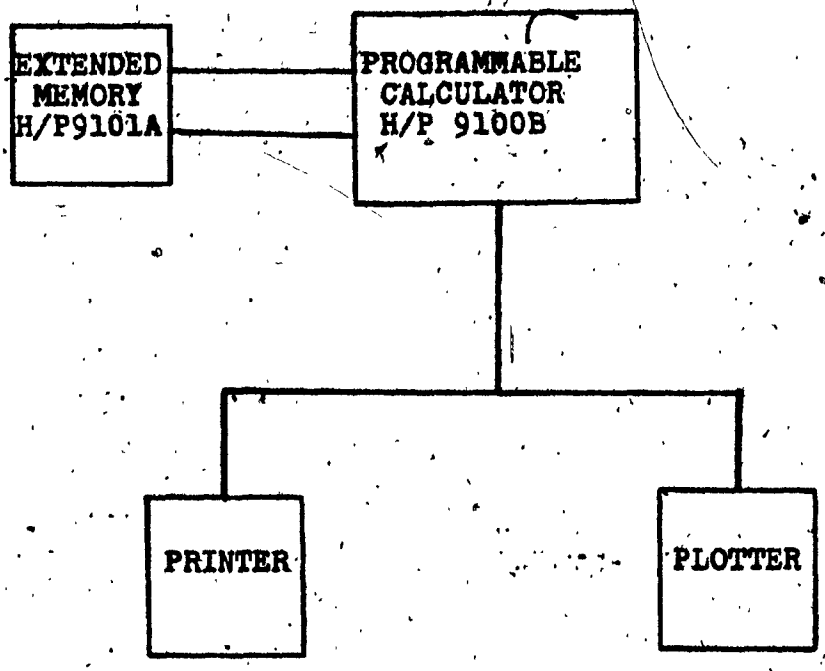


Figure 1.1

The Hewlett-Packard Programmable Calculator System.

the calculator system. The basic calculator, model 9100B, has a memory space of 28 registers. Each register can record 14 programming steps or store 1 numerical data. It is possible to load a program up to 512 programming steps into the calculator at the expense of data storage area. With the extended memory unit, the memory size is increased by 248 registers, totalling up to over 3400 programming steps. The programming techniques used in this thesis call for the storage of the involved sub-programs in the first half of the extended memory unit memory space and reserve the second half for data manupilation and storage. The sub-programs are entered from magnetic cards to the calculator via a card reader built in the calculator. The program in the calculator is then transferred to the extended memory unit for storage by the command, 'X', FMT, FMT, where 'X' is a numerical number between 0 and 99 to be given to the program being stored for identification. The command: 'X', FMT, GO TO, will re-call the program P'X' from the memory area to be loaded into the calculator memory area for program execution. This command can be either a programming step in a program or initiated from the calculator keyboard. In this way sub-programs can be called by another program.

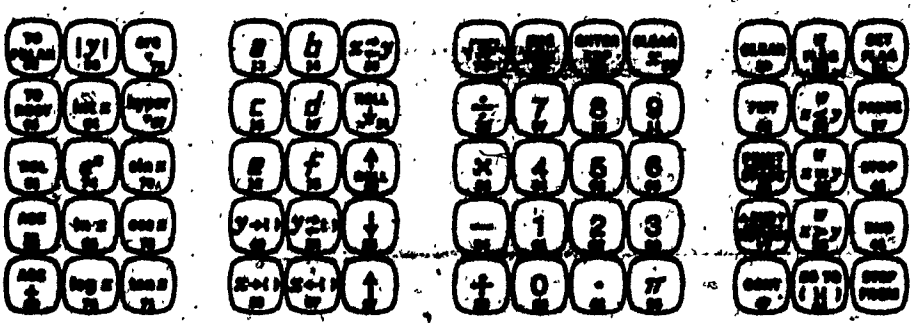
The printer uses a heat sensitive paper to record

the data on the calculator display system. Depending on the activation of the printer, any and all of the data in the calculator X-Y-X registers can be printed.

The plotter takes in the values in the X- and Y-registers and plots a point on the plotter table which holds the graph paper in place electro-statically. The coordinates of the point is in accordance with the values in the X- and Y-registers. A value of 500 will cause the plotter pen to move a distance of one inch along the direction of the axis (X-register value controls the X axis displacement and Y-register value controls the Y-axis displacement). The pen of the plotter will be activated by either of the commands: FMT UP or FMT DOWN. The first command will cause the pen to leave the paper surface and move to the coordinate point described by the values of the X-Y registers. The second command will cause the pen to move from its present position to the new position described by the X-Y register current values without leaving the paper surface. In this manner, a straight line is formed. The curves so generated by this plotter is actually composed of small segments of straight lines.

Fig. 1.2 shows the calculator keyboard as well as the key codes representing the programming steps.

9100B KEY CODES



00	0	13	a	26	ENTER EXP	41	STOP	54	SET FLAG	67	hyper •				
01	1	14	b	27	↑	42	PRT	55	|y|	67	x<(-)				
02	2	15	c	30	x≷y	43	R/S	56	π	70	sin x				
03	3	16	d	31	roll ↓	44	GO TO ( ) ( )	57	PAUSE	71	tan x				
04	4	17	e	32	GTO ENDS	45	POINT	60	ADD +	72	cos •				
05	5	20	CLEAR	33	+	46	SPACE	61	SCI	73	cos x				
06	6	21	•	34	−	47	END	62	TO POLAR	74	e^x				
07	7	22	roll ↑	35	÷	47	CONTINUE	63	ADD —	75	log x				
10	8	23	x<(-)	36	×	50	if x=y	64	INT x	76	$\sqrt{x}$				
11	9	24	y≷(-)	37	CLEAR x	52	if x<y	65	ln x	77	ABS				
12	E	25	↓	40	y<(-)	53	if x>y	66	TO HMS	77	RANDOM				

Figure 1.2

The Hewlett-Packard Programmable Calculator Model 9100B keyboard and key codes.

CHAPTER 2

CASCADED CIRCUIT ANALYSIS AND PROGRAM FORMULATION

2.1 General analysis of cascaded circuit topology

Consider the circuit of Fig. 2.1 with N cascaded circuit blocks. It can be shown that the circuit can be described by a graph of N+1 nodes and 2N+1 branches. A detailed solution of this circuit would require the establishment and simultaneous solution of the following equations:

. Kirchoff's voltage law, N equations;

$$[P_c^t] \cdot V_i = 0 \quad i=1,2, \ldots N \qquad (2.1.1)$$

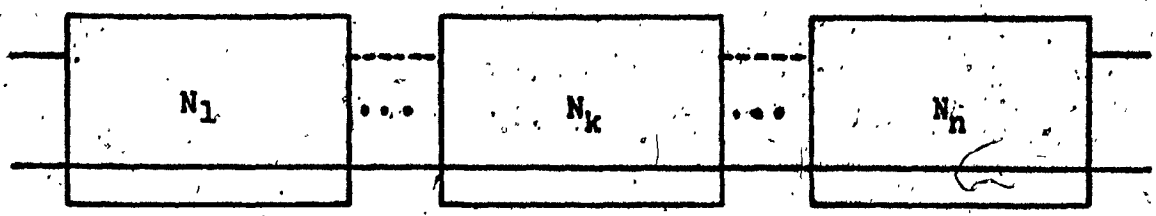
. Kirchoff's current law, 2N+1 equations.

$$[S_o^t] \cdot V_j = 0 \quad j=1,2,\ldots.2N+1 \qquad (2.1.2)$$

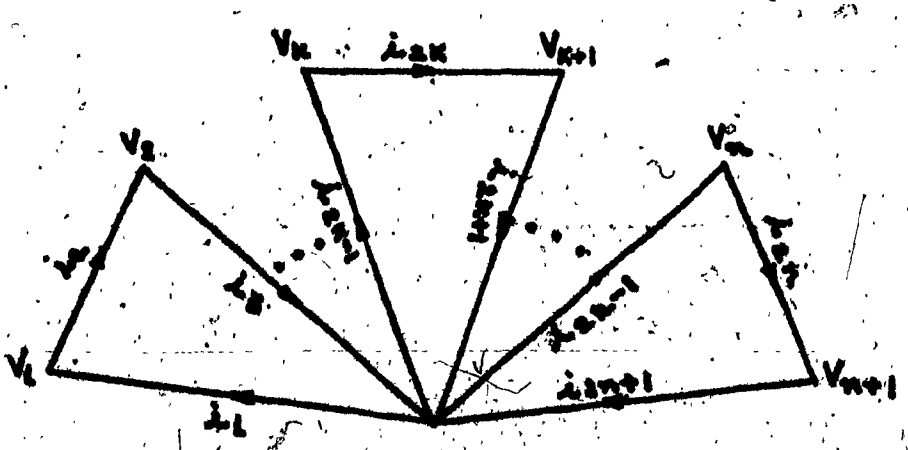
. Generalized Ohm's law for the branch elements, 2N+1 equations.

$$V_i - Z \cdot I_i = 0 \qquad (2.1.3)$$

where V_i and I_j are branch voltage and current vectors, P_c is tie-set matrix, S_o is cut-set matrix, and Z is generalized impedance matrix of the circuit.



(a) Cascaded circuit consisting of N circuit blocks.



(b) Graph representation of the above circuit.

Figure 2.1

General cascaded circuit topology

From the above equations, N+1 independent equations can be formed.

Although it is routine to solve such a system even for a large size of N in a modern computer by modern computer aides circuit design technique[3], it will be definitely beyond the memory size and capacity of the present desk top programmable calculator. Since in most cascaded circuits, only the terminal V-I relations are of interest, a substantial memory size saving can be achieved if the circuit is to be analysed specifically for the input and output voltages and currents only. This analysis can be most efficiently achieved through the use of Chain Matrix circuit characterization approach*.

Consider the circuit of Fig. 2.2, consisting of two cascaded circuits, each characterized by the respective chain matrices, A_1 and A_2,

$$\begin{bmatrix} V_{i1} \\ I_{i1} \end{bmatrix} = A_1 \begin{bmatrix} V_{o1} \\ -I_{o1} \end{bmatrix} \qquad (2.1.4)$$

$$\begin{bmatrix} V_{i2} \\ I_{i2} \end{bmatrix} = A_2 \begin{bmatrix} V_{o2} \\ -I_{o2} \end{bmatrix} \qquad (2.1.5)$$

* It should be noted that other methods such as conversion to T or π networks would involve matrix inversion, which may give rise to more errors than simple multiplication.

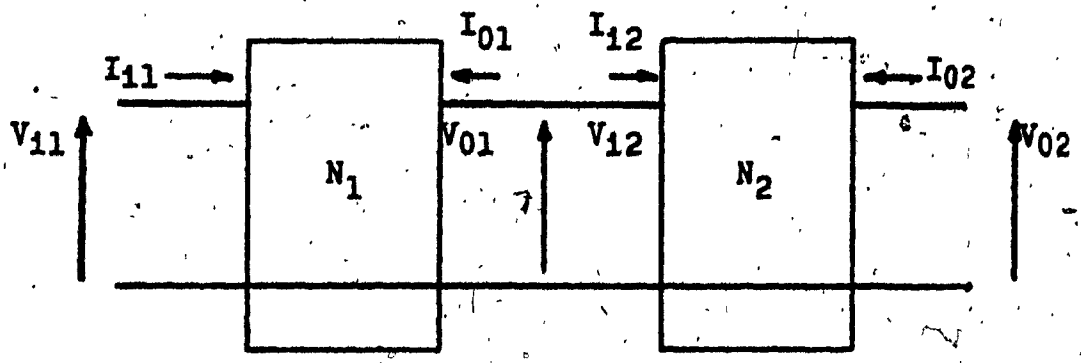


Figure 2.2
Terminal V-I relations in a network consisting of two cascaded circuit blocks.

it is straight forward to demonstrate that

$$\begin{bmatrix} V_{i1} \\ I_{i1} \end{bmatrix} = A_1 \cdot A_2 \begin{bmatrix} V_{o2} \\ -I_{o2} \end{bmatrix} \qquad (2.1.6)$$

Generalizing to a circuit consisting of N cascaded circuits, the terminal V-I relations can be written as

$$\begin{bmatrix} V_{i1} \\ I_{i1} \end{bmatrix} = \prod_{k=0}^{N} A_k \cdot \begin{bmatrix} V_{oN} \\ -I_{oN} \end{bmatrix} \qquad (2.1.7)$$

$$= A_T \cdot \begin{bmatrix} V_{oN} \\ -I_{oN} \end{bmatrix} \qquad (2.1.8)$$

The overall circuit is therefore represented by a single matrix, A_T, if only terminal V-I's: V_{i1}, I_{i1}, and V_{oN}, I_{oN} are of interest.

In the numerical calculation process, successive chain matrix multiplication will be performed to obtain the final chain matrix, A_T. This approach forms the basis for the development of both time and frequency domain circuit analysis programs. The terminal V-I relations will be derived accordingly from A_T.

2.2 Circuit analysis using chain matrix approach

A circuit chain matrix, A, defined as:

$$A = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \qquad (2.2.1)$$

can be computed using the following definitions:

$$a_{11} = \left(\frac{V_o}{V_i}\right)^{-1}, \quad I_o = 0 \qquad (2.2.2)$$

$$a_{12} = \left(\frac{-I_o}{V_i}\right)^{-1}, \quad V_o = 0 \qquad (2.2.3)$$

$$a_{21} = \left(\frac{V_o}{I_i}\right)^{-1}, \quad I_o = 0 \qquad (2.2.4)$$

$$a_{22} = \left(\frac{-I_o}{I_i}\right)^{-1}, \quad V_o = 0 \qquad (2.2.5)$$

In order to apply the chain matrix circuit analysis technique to a large network consisting of many circuit blocks, the only requirement is that the network can be subdivided into basic circuit blocks that can be cascaded together to form the original circuit. Circuits consisting of parallel or series feedback networks will not be suitable for this analysis although they can be manipulated using a combination of impedance and admittance matrix techniques in conjunction with the chain matrix approach.

The chain matrices for the basic circuit blocks to be used in this program may be derived easily and the results are listed as follows:

. Lumped elements

* "Series" connection (Fig. 2.3a)

$$A = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \qquad (2.2.6)$$

where Z is the impedance of the element

* "Shunt" connection (Fig. 2.3b)

$$A = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \qquad (2.2.7)$$

where Y is the admittance of the element

. Transmission line distributed parameters

* Cascaded connection (Fig. 2.3c)

$$A = \begin{bmatrix} \cos \beta l & j Z_o \sin \beta l \\ \frac{(\sin \beta l)}{j Z_o} & \cos \beta l \end{bmatrix} \qquad (2.2.8)$$

where β = propagation constant = ω/v
l = length of transmission line
Z_o = characteristic impedance of the transmission line
v = velocity of wave propagation

* "Series" and "Shunt" connections

The chain matrices for the series and shunt connections of the transmission line are the same for that of the lumped elements with the following definitions of Z and Y:

Short circuit terminated transmission line

"Series" connected (Fig.2.3d)

$$Z = j\, Z_o \tan \beta \ell \qquad (2.2.9)$$

"Shunt" connected (Fig. 2.3e)

$$Y = -j\, Y_o \cot \beta \ell \qquad (2.2.10)$$

Open circuit terminated transmission line

"Series" connected (Fig. 2.3.f)

$$Z = -j\, Z_o \cot \beta \ell \qquad (2.2.11)$$

"Shunt" connected (Fig. 2.3g)

$$Y = j\, Y_o \tan \beta \ell \qquad (2.2.12)$$

Two-port networks (Fig. 2.3h)

* Transistor

The active device is represented by its hybrid π model with the chain matrix as follows:

$$A = \begin{bmatrix} \dfrac{(1+j\omega C_{\mu} r_{b_2})}{(1-g_m r_{b_2})+j\omega C_{\mu} r_{b_2}} & \dfrac{r_{b_2}}{(1-g_m r_{b_2})+j\omega C_{\mu} r_{b_2}} \\ \dfrac{(1+j\omega C_{\mu} r_{b_2}) g_m}{(1-g_m r_{b_2})+j\omega C_{\mu} r_{b_2}} & \dfrac{1+j\omega C_{\mu} r_{b_2}}{(1-g_m r_{b_2})+j\omega C_{\mu} r_{b_2}} \end{bmatrix} \qquad (2.2.13)$$

where g_m = transconductance
r_{b_2} = collector to base resistance
C_{μ} = collector to base capacitance

the base-to-emitter resistance, r_{π}, and the collector-to-emitter resistance, r_o, are not included in the above matrix as they can be considered as additional cascade blocks of shunt resistances of values r_{π} and r_o.

* Scattering parameter circuit characterization

The scattering parameters are converted into chain matrix by a sub-routine in the program, and the resulting chain matrix dealt with in the regular manner. Two sets of scattering parameters at two different frequencies are needed in order to interpolate the scattering parameters between the two frequencies. This is calculated to provide swept frequency analysis capability even for matrix input(see Fig. 2.3i)

* Inverter (Fig. 2.3j)

$$A = \begin{bmatrix} 0 & K \\ 1/K & 0 \end{bmatrix} \qquad (2.2.14)$$

where K = inverter scaling factor

* Ideal transformer (Fig. 2.3k)

$$A = \begin{bmatrix} 1/N & 0 \\ 0 & N \end{bmatrix} \qquad (2.2.15)$$

where N = transformer turn ratio

All the above circuit blocks are acceptable circuit elements in the frequency domain circuit analysis program.

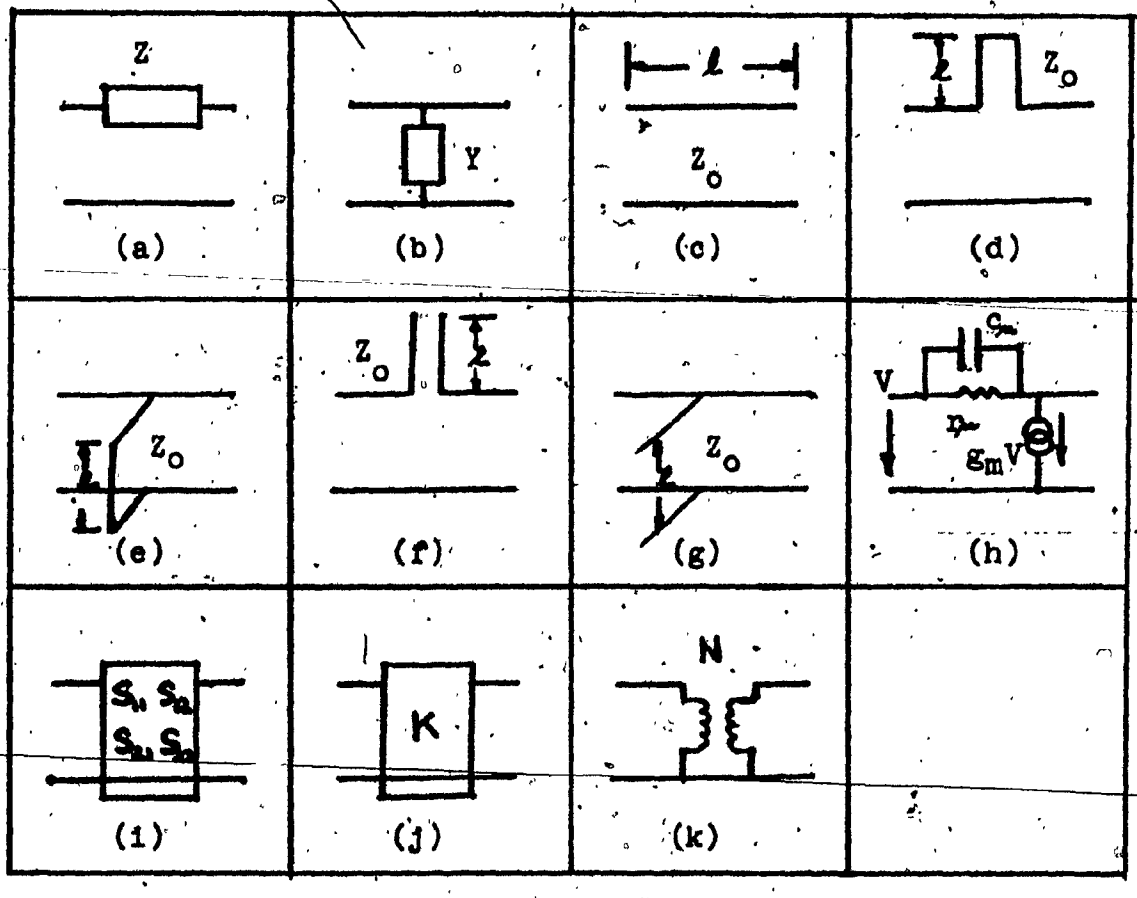


Figure 2.3

Circuit blocks used in the analysis

but only the lumped circuit elements are permissible in the time domain circuit analysis program.

After obtaining the overall chain matrix, the desired output function(s) can be found. The effects of the source and load impedances, Z_S and Z_L may be derived[4], but the results are listed below:

. Input impedance, Z_{in}

$$Z_{in} = \frac{a_{11}Z_L + a_{12}}{a_{21}Z_L + a_{22}} \qquad (2.2.16)$$

. Output impedance, Z_{out}

$$Z_{out} = \frac{a_{22}Z_S + a_{12}}{a_{21}Z_S + a_{11}} \qquad (2.2.17)$$

. Voltage transfer function, A_v

$$A_v = \frac{Z_L}{a_{11}Z_L + a_{12}} \qquad (2.2.18)$$

. Reflection coefficient Γ

$$\Gamma = \frac{Z - Z_o}{Z + Z_o} \qquad (2.2.19)$$

where Z_o = system reference impedance.

. Voltage standing wave ratio, VSWR

$$VSWR = \frac{1 + \Gamma}{1 - \Gamma} \qquad (2.2.20)$$

2.3 The frequency domain circuit analysis program

The fundamental techniques used in this program for circuit analysis at any given frequency is based on the successive multiplication of the chain matrices as discussed in section 2.1.

At a given frequency, the numerical values of the circuit chain matrices are computed and complex numbered matrix multiplication performed. The end product of this process is a 2 X 2 chain matrix consisting of the four complex numbers representing a_{11}, a_{12}, a_{21}, and a_{22}. The required output function(s) will be computed according to the equations in section 2.2.

At the conclusion of the calculation, the result will be presented (either printed or plotted) before proceeding to the next frequency for analysis. The new frequency is obtained by incrementing the existing frequency with a pre-determined incremental frequency. This process is repeated until the band edge frequency is reached. At that time, the total circuit analysis is completed.

2.4 Time domain circuit analysis program

In contrast to the frequency domain analysis in which the values of the response function are computed for each frequency, the purpose of the time domain analysis program is to compute the response time function, r(t), of a network for a given excitation, e(t).

Consider a system, described by the system function, H(s), the response in complex frequency domain, R(s), is related to the excitation, E(s), by

$$R(s) = H(s)E(s) \qquad (2.4.1)$$

where R, H, and E are functions of a complex variable, $s = \sigma + j\omega$.

Let H(s) be represented by a ratio of two polynomials:

$$H(s) = \frac{\sum_{n=0}^{N} a_n s^n}{\sum_{m=0}^{M} b_m s^m} \qquad (2.4.2)$$

or

$$\sum_{m=0}^{M} b_m s^m R(s) = \sum_{n=0}^{N} a_n s^n E(s) \qquad (2.4.3)$$

Performing inverse Laplace transform on both sides of equation 2.4.3 and restricting the analysis to initially relaxed systems only, we have:

$$\sum_{m=0}^{M} b_m \left(\frac{d}{dt}\right)^m r(t) = \sum_{n=0}^{N} a_n \left(\frac{d}{dt}\right)^n e(t) \qquad (2.4.4)$$

Let the derivatives of a function, X(t), be defined by the backward difference technique[5],

$$\left.\frac{dX}{dt}\right|_{t=KT} = \frac{X(KT) - X[(K-1)T]}{T}$$

$$\left.\frac{d^2X}{dt^2}\right|_{t=KT} = \frac{\left.\frac{dX(KT)}{dt} - \frac{dX[(K-1)T]}{dt}\right.}{T}$$

$$= \frac{X(KT)-2X[(K-1)T]+X[(K-2)T]}{T^2}$$

$$\vdots$$

$$\left.\frac{d^nX}{dt^n}\right|_{t=KT} = \frac{1}{T^n}\sum_{n=0}^{N} \frac{N!\, X[(K-n)T](-1)^n}{(N-n)!\; n!} \qquad (2.4.5)$$

Substituting the equation 2.4.5 to equation 2.4.4, the differential equation (equation 2.4.4) becomes an algebraic equation:

$$\sum_{m=0}^{M} \frac{b_m}{T^m} r(KT) + \sum_{m=1}^{M} \frac{b_m m!}{T^m} \sum_{i=1}^{m} \frac{r[(K-i)T](-1)^i}{(m-i)!\,i!}$$

$$= \sum_{n=0}^{N} \frac{a_n e(KT)}{T^n} + \sum_{n=1}^{N} \frac{a_n n!}{T^n} \sum_{j=1}^{n} \frac{e[(K-j)T](-1)^j}{(n-j)!\,j!} \qquad (2.4.6)$$

From this equation, r(KT) can be solved in terms of r[(K-1)T], r[(K-2)T],....., r[(K-M)T], and e(KT), e[(K-1)T], e[(K-2)T], ..., e[(K-N)T].

$$r(KT) = \left[\sum_{n=0}^{N} \frac{a_n}{T^n} e(KT) + \sum_{n=1}^{N} \frac{a_n n!}{T^n} \sum_{j=1}^{n} \frac{e[(K-j)T](-1)^j}{(n-j)!\, j!} - \sum_{m=1}^{M} \frac{m! b_m}{T^m} \sum_{i=1}^{m} \frac{r[(K-i)T](-1)^i}{(m-i)!\, i!}\right] \frac{1}{\sum_{m=0}^{M} b_m/T_m} \qquad (2.4.7)$$

Based on equation 2.4.7, r(KT) can be numerically evaluated by a programmable calculator for each value of KT.

Similar to the frequency domain analysis program, the time domain analysis technique also relies on matrix multiplication. The difference is that the matrix elements are polynomial functions instead of complex numbers. Though this does not present any theoretical difference, in practice, the programming difficulty is very much increased due to the large amount of data required to be stored.

CHAPTER 3

FREQUENCY DOMAIN CIRCUIT ANALYSIS PROGRAM

3.1 Program development

Similar to all other types of circuit analysis programs, the basic structure of the program consists of:

- Input sub-program to accept circuit elements and circuit parameter informations.
- Circuit analysis sub-program to perform the numerical calculation.
- Output function computation sub-programs.
- Output presentation sub-routines.

Shown in Fig. 3.1 is the simplified overall flow-chart. Listed with each block are the sub-programs (identified by the program numbers) performing such functions. Figure 3.2 is a memory map of the extended memory to show all the sub-program storage locations, data storage area, and computation work area.

3.1.1 Circuit data input sub-program

The input sub-program provides a convenient and

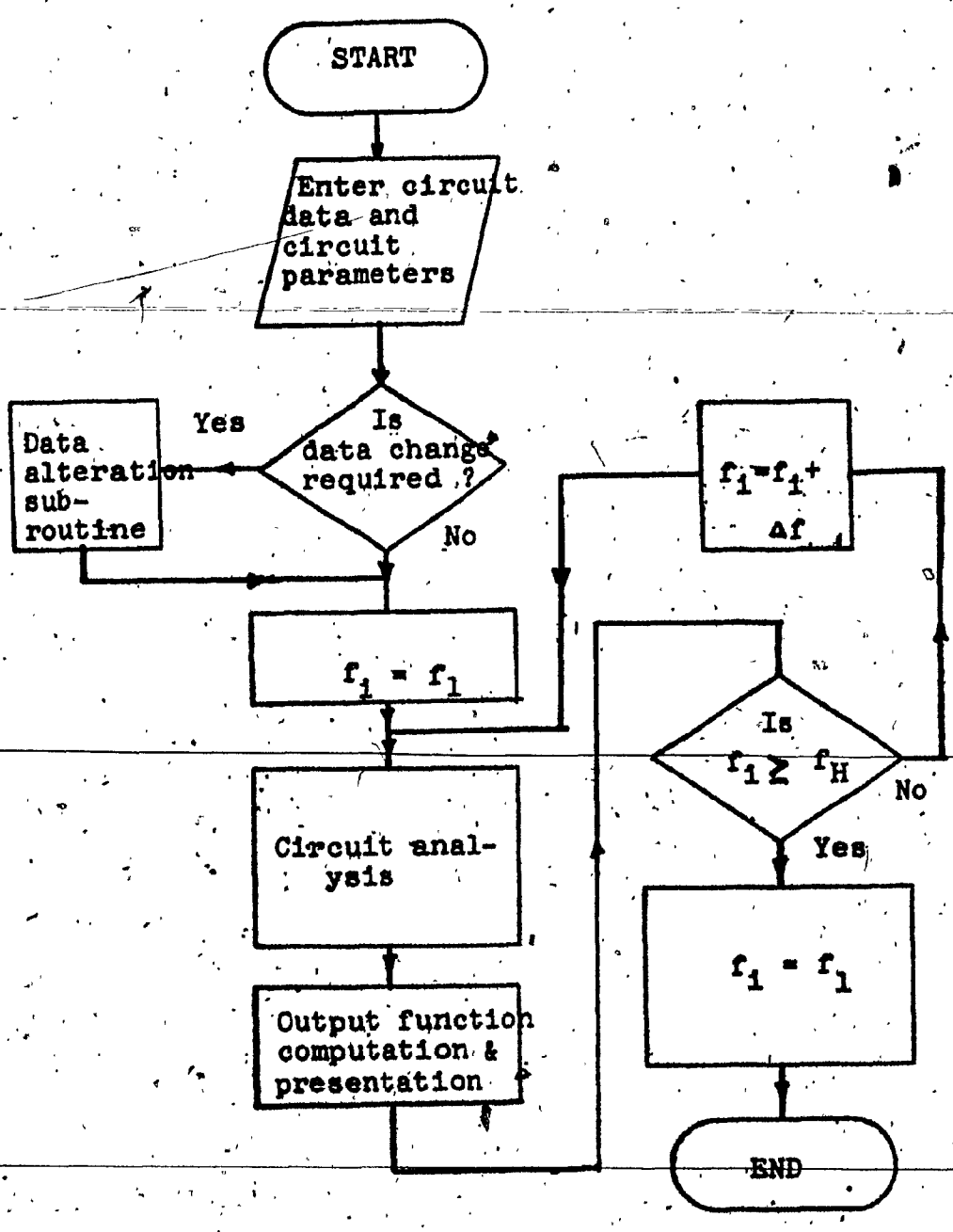


Figure 3.1

Simplified overall flow-chart of the Frequency Domain Circuit Analysis Program

Title FREQUENCY DOMAIN CIRCUIT ANALYSIS Date FEB. 1975 Page 1 of 1

PROGRAM MEMORY MAP Name C.H.C.I.I

Figure 3.2

9101A MEMORY MAP

0		50		100		150		200	ΔX FOR
1		51		101		151		201	y. PLOTTER
2	P1:	52		102		152		202	Δy
3		53		103		153		203	
4	CIRCUIT	54		104		154		204	
5	ANALYSIS	55	CIRCUIT ELEMENT	105		155		205	R_S
6	INITIALIZATION	56	CHAIN MATRIX	106		156		206	R_L
7		57	FORMATION AND	107		157		207	OUTPUT BLOCK INDEX
8		58	OUTPUT FUNCTION	108		158		208	CIRCUIT BLOCK WORK
9		59	COMPUTATION	109		159		209	N=TOTAL NO. OF CKT.
10		60	PROGRAMS	110		160		210	$R_e A_{11}$
11		61	AND PLOTTING	111		161		211	MATRIX $I_m A_{11}$
12		62	SUB-ROUTINES	112		162		212	MULT. $R_e A_{12}$
13		63	TO BE LOADED	113		163		213	WORK $I_m A_{12}$
14		64	AS REQUIRED	114		164		214	AREA $R_e A_{21}$
15		65		115		165		215	$I_m A_{21}$
16	P2:	66		116		166		216	$R_e A_{22}$
17		67		117		167		217	$I_m A_{22}$
18	COMPLEX	68		118		168		218	$R_e B_{11}$
19	NUMBERED	69		119		169		219	$I_m B_{11}$
20	MATRIX	70		120		170		220	$R_e B_{12}$
21	MULTIPLICATION	71		121		171		221	$I_m B_{12}$
22		72		122		172		222	$R_e B_{21}$
23		73		123		173		223	$I_m B_{21}$
24		74		124	CIRCUIT DATA	174	CIRCUIT DATA	224	$R_e B_{22}$
25		75		125	STORAGE	175	STORAGE	225	$I_m B_{22}$
26		76		126		176		226	$R_e C_{11}$
27		77		127		177		227	$I_m C_{11}$
28	P3:	78		128		178	#4	228	$R_e C_{12}$
29	COMPLEX ADD	79	(NO DIVISION	129		179		229	$I_m C_{12}$
30	MULTIPLICATION	80	LINE BETWEEN	130		180		230	$R_e C_{21}$
31		81	PROGRAM	131		181		231	$I_m C_{21}$
32		82	MEMORY SPACE	132		182	#3	232	$R_e C_{22}$
33		83	AND DATA	133		183		233	$I_m C_{22}$
34	P4:	84	STORAGE IS	134		184		234	COMPLEX $R_e d_{11}$ R
35	DATA TRANSFER	85	GIVEN MORE	135		185		235	NO. MULT. $I_m d_{11}$ I
36	P5:	86	CIRCUIT BLOCKS	136		186		236	WORK $R_e d_{12}$ R
37	MATRIX DATA	87	CAN BE HANDED	137		187	#2	237	AREA $I_m d_{12}$ I
38	TRANSFER	88	IF SPACE	138		188		238	$R_e C_{11}$
39	P6:	89	ALLOWS.)	139		189		239	$I_m C_{11}$
40	INPUT DATA	90		140		190	CIRCUIT	240	$R_e E_{11}$
41	ALTERATION	91		141		191	BLOCK	241	$I_m E_{11}$
42	P8:	92		142		192	#1	242	$R_e f_{11}$
43	NULL MATRIX	93		143		193	DATA FOR	243	$I_m f_{11}$
44		94		144		194	OUTPUT	244	Δf FREQUENCY
45	P9:	95		145		195	FUNCTION	245	f_1 INFORMATION
46	UNITY MATRIX	96		146		196	COMPUTATION	246	f_2
47		97		147		197		247	f_n
48		98		148		198			
49		99		149		199	X_n DATA		

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systemmatic method by which a circuit to be analysed can be described. Other informations, such as the desired output function(s), the type of output presentation and the frequencies between which analysis is to be performed, are also entered.

The sub-program accepts N, which specifies the total number of circuit blocks composing the overall circuit. The information for each circuit block are entered next. A code numbering system is used to designate whether the circuit element described in the circuit block is connected in "series", in "shunt", or in cascaded configuration. Listed below are the codes:

Connection	Code
Series	1
Shunt	2
Cascaded	3

The circuit type in each circuit block is also represented by codes:

Circuit type	Code
Resistor	1
Series connected R-L-C	2
Parallel connected R-L-C	3
Open circuit terminated transmission line	4
Short circuit terminated transmission line	5
Cascaded connected transmission line	6

Circuit type	Code
Transformer	7
Inverter	8
Transistor hybrid model	9
Scattering parameters defined circuit block	3

The circuit element values in the blocks can be described by up to three numbers. For example, a series R-L-C will be specified by: resistance in ohms, inductance in henries, and capacitance in farads. Table 3.1 summarizes all the circuit types, their codes and the circuit element data entry format.

The specification of the desired output function(s) and the presentation formats will be entered after the completion of the input data entry. A code numbering system is also used. The present sub-programs provide computation for several commonly used functions. However, additional user-defined functions can be added to the sub-routines if necessary.

Output function	Code
Input impedance (with output port terminated by R_L)	1
Output impedance (with input port terminated by R_S)	2

* No confusion between the scattering parameters defined circuit block and the parallel connected R-L-C circuit may exist, because the first circuit block can be used only in cascaded connection, and the second block used only in series or shunt connection.

Circuit connection code (P)

"Series" 1
"Shunt" 2
"Cascade" 3

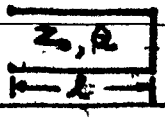
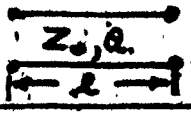
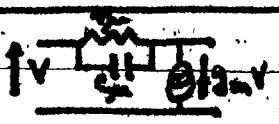
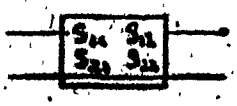
Circuit type	Description	Code (Q)	Data entry sequence at X-register display 1	2	3
	Resistor (Ohms)	1	R	0	0
	Series R-L-C. (Ohms, henries, farads)	2	R	L	C
	Parallel R-L-C. (Ohms, henries, farads)	3	R	L	C
	Open circuit terminated transmission line. (equivalent length in free space, inches, line impedance, ohms, Q factor)	4	1	Z_o	Q
	Short circuit terminated transmission line.	5	1	Z_o	Q
	Cascaded transmission line.	6	1	Z_o	Q
	Transformer	7	N		
	Inverter	8	K		
	Transistor, Hybrid model.	9	r	c	g_m
	S-parameters input	3	f_a	f_b	Z_o (See Appendix III for details.)

TABLE 3.1

List of acceptable circuit type and circuit connection codes together with proper input formats.

Output function	Code
Transducer power gain (phase and magnitude in db)	3
Voltage standing wave ratio	4
Reflection coefficient	5
Overall chain matrix	6

The above output functions can be presented using a calculator built-in printer, an X-Y plotter, or both. When necessary, an output function can be specified to be computed but the result not presented. Instead, it is used to compute other output functions. An example of this situation is illustrated in the calculation of input reflection coefficient. In this case, the input impedance is first computed. Without calling for an output, the result is immediately used to compute the reflection coefficient defined by the Z_{in} just obtained. This final result is displayed. When the plotter output is specified, provision is given to enter the X-Y coordinates of the origin and the X-Y axes scaling factors. The output functions and presentation options codes, together with the output formats are summarized in table 3.2.

Next to be specified in the input program are the source and load resistances. An entry of 0 or very large value to represent short or open circuit is also acceptable.

Output presentation options

Printout:	Impedances	1
	Frequency response	2
	Smith chart	3
Plotter:	Frequency response	4

Output function	Description	Code	Printout format X	Y	Z
Input impedance, Z_{in}	$Z_{in}=V_{in}/I_{in}$, out-terminated by R_L	1	$Re(Z_{in})$	$Im(Z_{in})$	Freq.
Output impedance, Z_{out}	$Z_{out}= V_o/I_o$, input terminated by R_S	2	$Re(Z_{out})$	$Im(Z_{out})$	Freq.
Transducer power gain	$T = P_o/P_{avail}$	3	T,(dB)	Angle, degree	Freq.
VSWR	Voltage standing wave ratio	4	VSWR	[illegible]o	Freq.
Reflection coefficient	$\Gamma = (Z-Z_o)/(Z+Z_o)$	5	$Re(\Gamma)$	$Im(\Gamma)$	Freq.
Overall Chain Matrix, A_T	$A_T = \prod_{i=1}^{N} A_i$	6	$Re(a_{ij})$	$Im(a_{ij})$	Freq.

TABLE 3.2

Available output functions, presentation options, and printout data interpretation.

The information for frequency sweeping is provided by specifying the initial frequency, final frequency, and the size of the frequency increment. With this information entered, the circuit elements and parameters entry procedure is completed. At this point, a provision is made to allow correction of any input data. This is accomplished by first locating the memory address of the data and re-enter the corrected value into this address. A sub-routine is prepared for this operation.

The overall flow-chart of the input program is shown in Fig. 3.3. Since this input program is used only once(to enter circuit data at the beginning of the program execution), and is not re-called later, it is not stored in the extended memory. This significantly optimizes the economical usage of the memory space. The programming steps are recorded on a magnetic card and is loaded to the desk-top calculator via a built-in card reader.

3.1.2 Circuit analysis sub-program

As discussed previously, circuit analysis is accomplished by successive matrix multiplication of all the chain matrices representing the cascaded circuit blocks. The

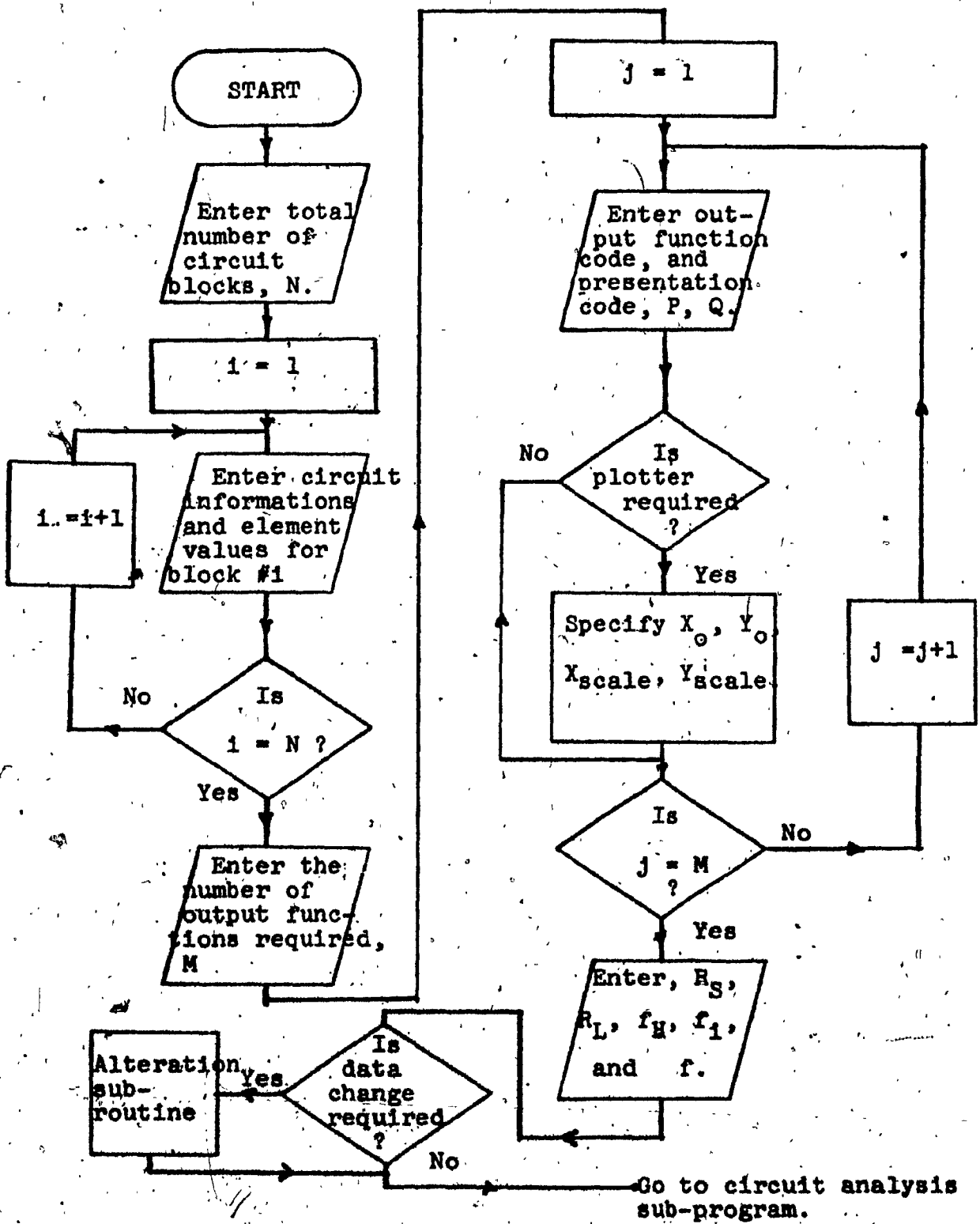


Figure 3.3

Flow-chart for Input Sub-program

heart of the circuit analysis sub-program, in this respect, is the sub-routine to perform complex numbered matrix multiplication and addition.

Depicted in the flow-chart in Fig. 3.4, a 2 X 2 matrix, A, is initially set to be unity matrix. The code describing circuit block #1 is examined. This code activates a sub-routine to form a chain matrix according to the circuit type, circuit element values and the frequency at which the circuit is evaluated. This matrix is designated as B. Matrix multiplication is performed on A and B with the result called C:

$$C = A \cdot B \qquad 3.1.1$$

The values of the matrix elements in A are subsequently replaced by C:

$$A = C \qquad 3.1.2$$

Successively, the chain matrices of circuit blocks #2, 3,...N are formed and multiplied to the up-dated value of matrix A. This process will stop after the N^{th} circuit block is executed. The final result in C represents the overall chain matrix A_T, and output function(s) may be derived from it.

After all the specified output functions are executed,

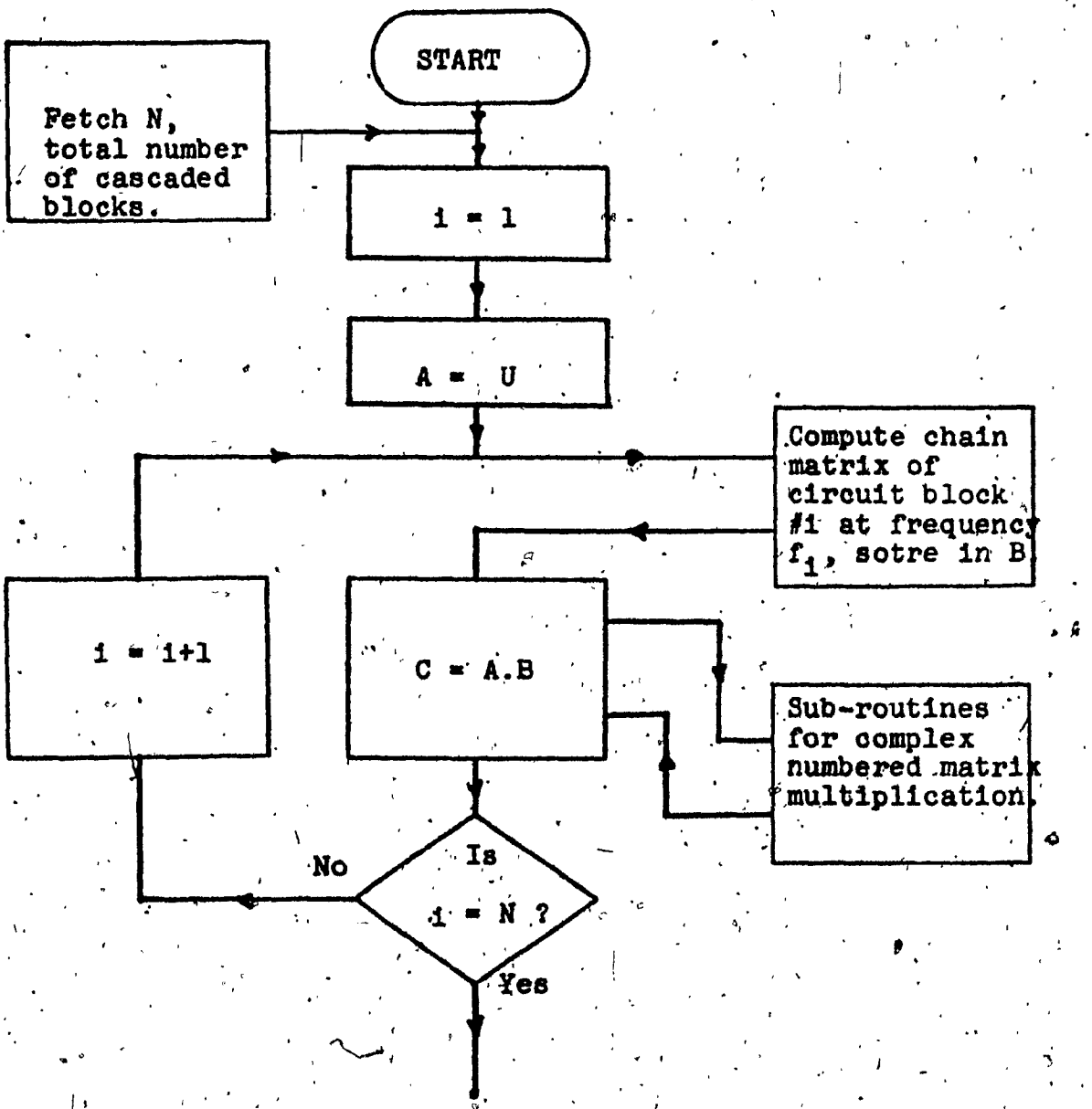


Figure 3.4

Flow-chart for Circuit Analysis Sub-program

control is returned to this sub-program for analysis at a new frequency, specified by advancing the existing frequency by a prescribed increment. This swept frequency analysis is carried on until the high band-edge frequency is reached. At this point, the execution of the overall program is completed.

3.1.3 Output function computation and data presentation sub-programs

This sub-program calculates the numerical values of the specified output functions using the overall chain matrix A_T obtained from the circuit analysis sub-program. The inclusion of the effects of the source and load resistances is accomplished using the equations in section 2.2. With the specified output computed, the result will be either printed, plotted, or both. When the plotted output presentation is required, special sub-programs will be activated to drive the plotter for a frequency response plot or Smith Chart plot.

When more than one output function are specified, each will be successively computed, and the output immediately presented before proceeding to the computation of the next output function. Due to the plotter limitations, though up to 5 functions can be executed, only one can be plotted and the rest printed by the printer.

The overall flow-chart is shown in Fig. 3.5

3.2 Program loading

The complete frequency domain circuit analysis program consists of several sub-programs. They can be divided into five catagories according to their functions:

- Circuit analysis sub-programs, composing of P1 - P6, P8 and P9.
- Circuit block chain matrix formation sub-routines, P11 - P15, P21 - P25, P33, P36 - P39, P90 - P91.
- Output function computation sub-programs, P41 - P46.
- Output presentation sub-routines, P51 - P54.
- Input data entry sub-program, P0. This sub-program is not to be stored in the extended memory unit.

It is not necessary to load all the sub-programs into the extended memory to have the system operative. The sub-programs performing circuit analysis are to be completely loaded to the extended memory unit. However, only the selected sub-programs to describe the circuit elements and compute the output functions are required. This selective loading technique significantly optimizes the economical usage of the much precious memory space. The table in Fig. 3.6

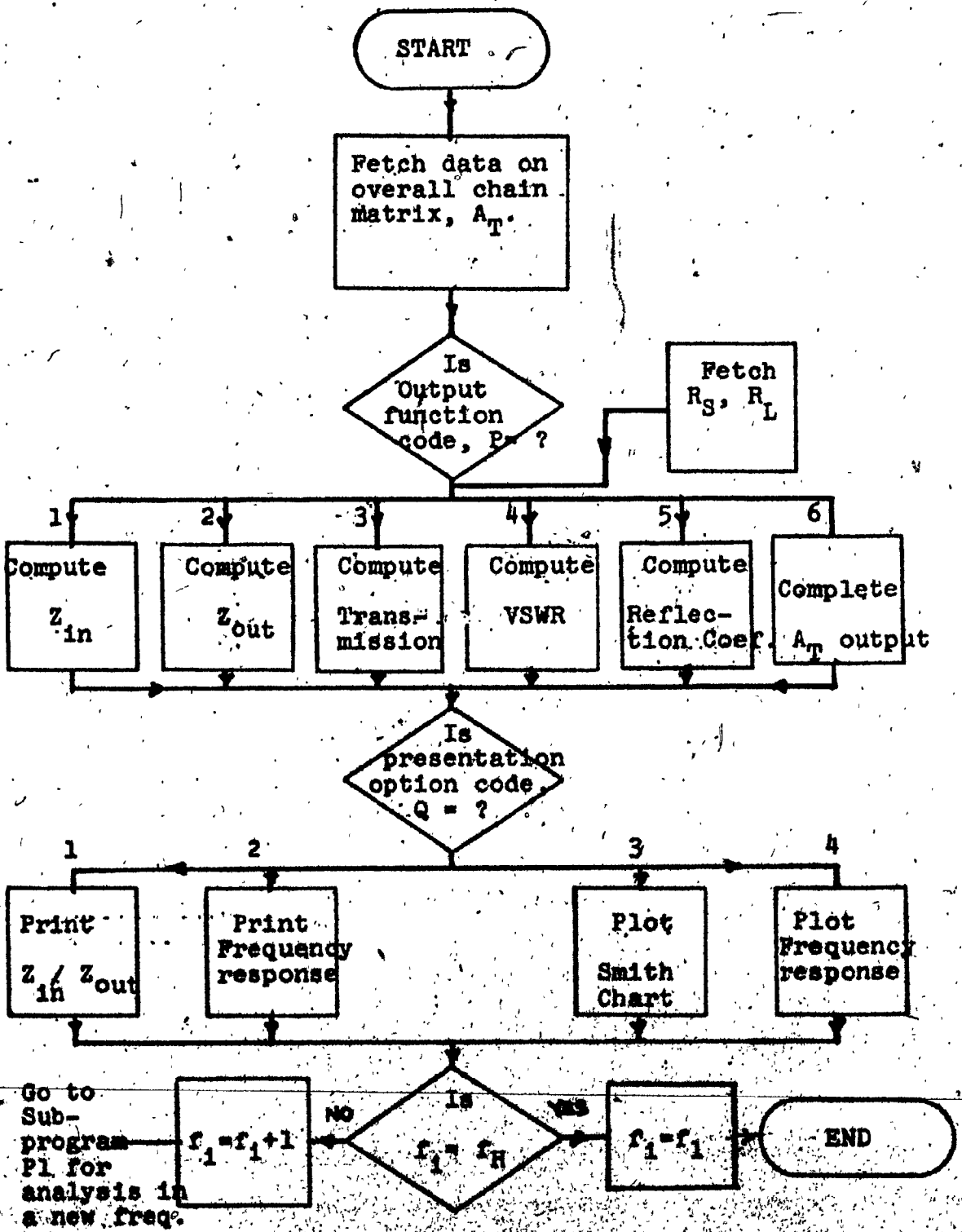
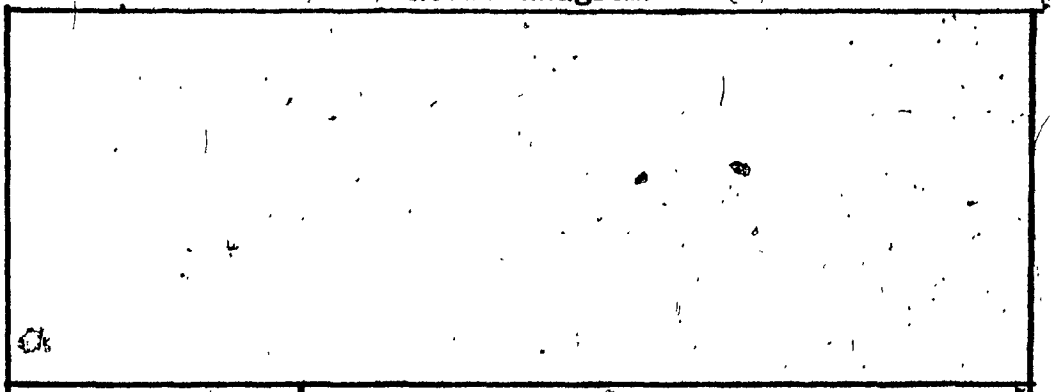


Figure 3.5

Flow-chart of Output Sub-program

Circuit diagram



Ckt. block No.		
Connection code		
Ckt. type code		
Element values	1	
	2	
	3	

Required output functions:

List all sub-programs to be entered to the calculator extended memory:

Other Informations

PRINT/PLOT Plot routine informations:

R_S = R_L= X_o = X_{scale}=

f_1 = Y_o = Y_{scale}=

f_2 = f=

Figure 3.6

Suggested Input data organization Table

gives a summary of the preliminary user preparation to organize the circuit data for more efficient and accurate circuit information entry to the program.

The following gives the program loading procedures:

File protect switch (extended memory unit): OFF.

Step	User action	Display X	Y	Z
1	Press: CLEAR, FMT, SET FLAG.	0	0	0
2	Enter: P1.			
3	Press: 1, FMT, FMT.	14	0	0
4	Enter: P2.			
5	Press: 2, FMT, FMT.	26	0	0
6	Enter: P3.			
7	Press: 3, FMT, FMT.	33	0	0
8	Enter: P4.			
9	Press: 4, FMT, FMT.	35	0	0
10	Enter: P5.			
11	Press: 5, FMT, FMT.	38	0	0
12	Enter: P6.			
13	Press: 6, FMT, FMT.	41	0	0
14	Enter: P8.			
15	Press: 8, FMT, FMT.	44	0	0
16	Enter: P9.			
17	Press: 9, FMT, FMT.	46	0	0
18	Enter the selected circuit block programs using the format: X, FMT, FMT. where X is the program identification number.			
19	Enter the selected output function subprograms using the format: Y, FMT, FMT. where Y is the program identification number.			
20	Enter the selected output presentation programs using the format: Z, FMT, FMT. where Z is the program identification number.			
21	File protect switch (extended memory unit): ON.			
22	Press: END.			
23	Enter: P0.			

The number displayed in the X-register in each instance indicates the total number of registers used in the extended memory unit. A correct display indicates that the sub-programs are properly stored. The program can be readily executed at the completion of the above loading procedures.

3.3 Program execution

Program execution can be effected using the following steps. The input data are expected to be arranged in the order according to the table of Fig. 3.6.

PLOTTER: ON.
PRINTER: WITH X-, Y-, Z- printouts ALL ON.
FLOATING/FIXED switch: optional position.
PROGRAM/RUN switch: RUN.

Step	User action	Display X	Y	Z
1	Press: END, CONTINUE.	1	1	0
2	Enter: N, total number of circuit blocks, into X-register.	N		
3	Press: CONTINUE. where i indicates data for circuit block #i are to be entered. i = 1, 2,....N.	i	i	i
4	Enter: Circuit connection code, P, into X-register, and circuit type code, Q, into Y-register. (refer to table 3.1 for values of P and Q).	P	Q	
5	Press: CONTINUE. the X-register display of "1" indicates the first element value of circuit block #i (i as displayed in Z-register) is to be entered into X-register.	1	PQ	i

Step		User action	Display X	Y	Z
5(continue)		The sub-program identification number, PQ, for circuit block #i is shown in Y-register. This sub-program PQ will form the chain matrix for this circuit block.			
6	Enter:	First element value for circuit block #i into X-register.	g_1		
7	Press:	CONTINUE.	2	PQ	i
8	Enter:	Second element value for circuit block #i into X-register.	g_2		
9	Press:	CONTINUE.	3	PQ	i
10	Enter:	Third element value for circuit block #i into X-register.	g_3		
11	Press:	CONTINUE.	i+1	i+1	i+1
	.	Steps 3 to 10 are repeated			
	.	for data entry for the #(i+1)			
	.	circuit block. This process is			
	.	repeated until data entry for			
	.	all the N circuit blocks are			
	.	completed.			
12	Press:	CONTINUE.	2	2	0
13	Enter:	Total number of outputs, M, into X-register.	M		
14	Press:	CONTINUE. The display of "j" reminds output function specification for #j output is to be entered. j = 1, 2,...M.	j	j	j
15	Enter:	Output function specification codes, R and S, into X- and Y-register respectively. R = Output presentation code. S = Output function code.	R	S	
16	Press:	CONTINUE. (If plotter output is not called for, go to 17d)	j+1	j+1	j+1
		(If plotter output is required, proceed to 17a)	2	2	1
17a	Enter:	X coordinate of origin in Y-register, X axis scaling factor, units/inch, in X-register.	X_{scale}	X_o	
17b	Press:	CONTINUE	2	2	2
17c	Enter:	Y coordinate of origin in Y-register, Y axis scaling factor, units/inch, in X-register.	Y_{scale}	Y_o	

Step		User action	Display X	Y	Z
17d	Press:	CONTINUE.	j+1	j+1	j+1
18	Enter:	Output function codes, R and S, for output function #(j+1). (repeat steps 15 to 17 as required until all M output options are defined.)			
19	Press:	CONTINUE.	3	3	0
20	Enter:	Source and load resistances, R_s, R_L, into Y- and X-register respectively.	R_L	R_S	
21	Press:	CONTINUE.	4	4	0
22	Enter:	High band-edge frequency, f_H, in Z-register, starting frequency, f_1, in Y-register, frequency increment, Δf, in X-register. Units of frequency: Hz.	Δf	f_1	f_H
23	Press:	CONTINUE.	1	6	6
24	Press:	If no correction is required, CONTINUE. Circuit analysis sub-programs are activated automatically.			
	Press:	If data correction is required, 6, CONTINUE.	6	6	6
25a	Enter:	Total number of corrections, K, in X-register.	K		
25b	Press:	CONTINUE. where "i" indicates the i^{th} correction is being made. i = 1, 2,..K.	i	i	i
25c	Enter:	Memory map address of data to be corrected in X-register.	memory map address		
25d	Press:	CONTINUE.	data (old)	data (old)	i
25e	Enter:	Corrected data in X-register.	data (new)		
25f	Press:	CONTINUE. (Steps 25b to 25f are repeated until all corrections are performed. At that time, circuit analysis sub-program will be automatically engaged.)	i+1	i+1	i+1

If at any time, data alteration is desired, steps 25a - 25f can be initiated by calling sub-routine P6:

6, FMT, GO TO, END, CONTINUE.

Also circuit analysis sub-program, P1, can be initiated by:

Press: 1, FMT, GO TO, END, CONTINUE.

After the circuit analysis sub-program, P1, is initiated, the calculator registers will periodically flash-display the circuit block number currently being executed. Data outputs are given at the completion of analysis at each frequency. This process continues until analysis at the highest frequency band-edge is performed. The program will stop automatically after that.

3.4 Circuit analysis examples

Two circuit analysis examples are given in this section. The first example deals with the frequency response of a inter-digital microwave frequency bandpass filter. The second example, which employs a transistor characterized by scattering parameters, demonstrates the analytic capability of the program even with matrix input.

3.4.1 A 6 GHz band-pass filter

Developed for use in a microwave receiver, this filter is an interdigital type having 7 resonators and input and output matching circuits designed using the procedures

of G. L. Matthaei[6].

The filter structure is shown photographically in Fig. 3.7. The circuit, modelled by transmission lines, is presented in Fig. 3.8

The procedures for program execution as described in section 3.3 are given for typical circuit blocks to demonstrate the use of the frequency domain circuit analysis program.

Input data entry

Step	User action		Display X	Y	Z
1	Press:	END, CONTINUE.	1	1	0
2	Enter:	Total number of cascaded circuit blocks, 18, into X-register.	18		
3	Press:	CONTINUE.	1	1	1
4	Enter:	Shunt connection code, 2, into X-register, and short circuit terminated line code, 5, into Y-register.	2	5	
5	Press:	CONTINUE.	1	25	1
6	Enter:	First circuit element: length of line in inches, 0.484 in. into X-register	0.484		
7	Press:	CONTINUE.	2	25	1
8	Enter:	Second circuit element: characteristic impedance, Z_o, 65.2 into X-register.	65.2		
9	Press:	CONTINUE.	3	25	1
10	Enter:	Third circuit element, Q factor of the line, 400 into X-register.	400		

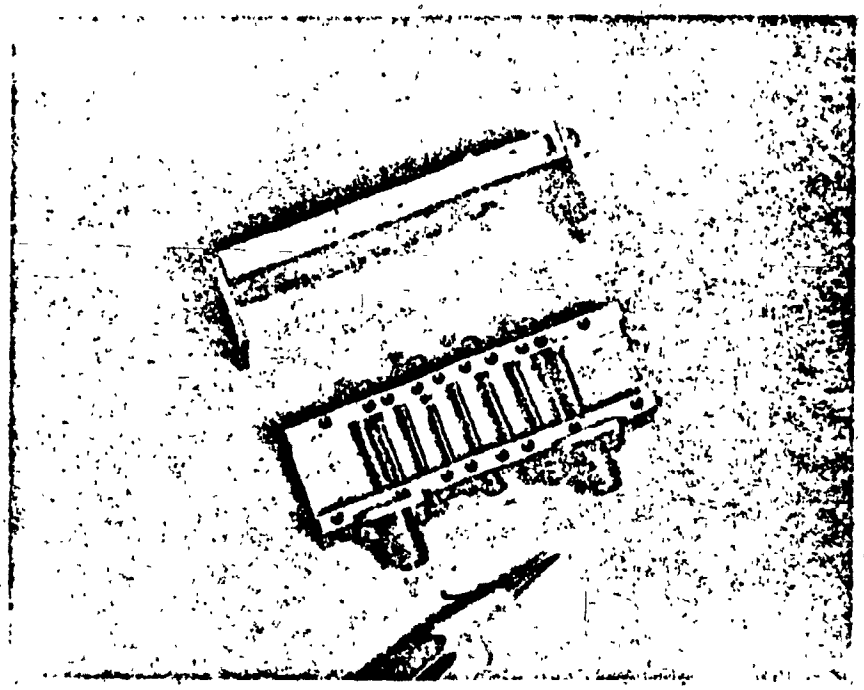
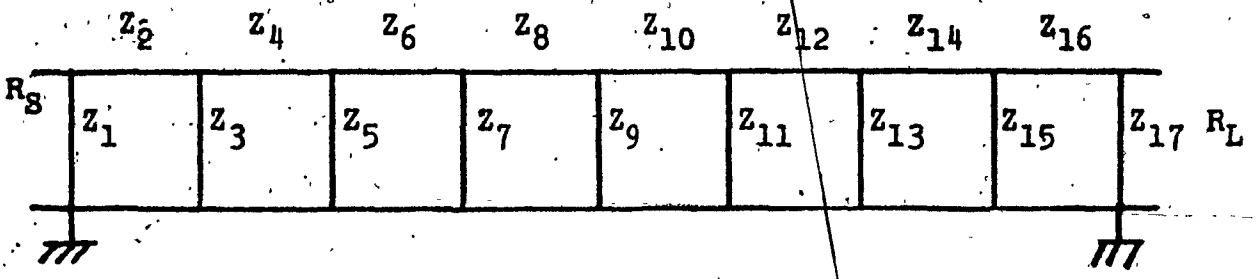


Figure 3.7

A 5.8 - 6.5 GHz interdigital
Bandpass filter



Lengths of all transmission lines: 0.484 inch (one-quarter wave length at 6.095 GHz)

Circuit element	Characteristic impedance, Z_o Ohms	Unloaded Q
Z_1, Z_{17}	65.2	400
Z_2, Z_{16}	214.2	1500
Z_3, Z_{15}	143.6	400
Z_4, Z_{14}	1046.4	1500
Z_5, Z_{13}	101.2	400
Z_6, Z_{12}	1421.5	1500
Z_7, Z_{11}	98.74	400
Z_8, Z_{10}	1500.8	1500
Z_9	98.43	400

Figure 3.8

Transmission line model of the microwave Interdigital Filter

Title Memory map for the Interdigital Bandpass Filter. Date Feb. 1975. Page 1 of 1
Name C. H. C. Li

Figure 3.9

9101A MEMORY MAP

0		50		100		150	98.74	200	2x10⁸
1		51	P_{25}	101		151	0.484	201	0
2	P_1	52		102		152	25	202	40
3		53		103		153	1500	203	
4		54		104		154	1500.8	204	
5		55		105		155	0.484	205	50
6		56		106		156	36	206	50
7		57	P_{36}	107		157	400	207	
8		58		108		158	98.43	208	
9		59		109		159	0.484	209	17
10		60		110		160	25	210	
11		61		111		161	1500	211	
12		62		112		162	1501.8	212	
13		63		113		163	0.484	213	
14		64		114		164	36	214	
15		65		115		165	400	215	
16		66		116		166	98.74	216	
17	P_2	67	P_{41}	117		167	0.484	217	
18		68		118		168	25	218	
19		69		119		169	1500	219	
20		70		120		170	14215	220	
21		71		121		171	0.484	221	
22		72		122		172	36	222	
23		73		123		173	400	223	
24		74		124		174	101.2	224	
25		75	P_{43}	125	400	175	0.484	225	
26		76		126	65.2	176	25	226	
27		77		127	0.484	177	1500	227	
28	P_3	78		128	25	178	10464	228	
29		79		129	1500	179	0.484	229	
30		80		130	214.2	180	36	230	
31		81	P_{44}	131	0.484	181	400	231	
32		82		132	36	182	143.6	232	
33		83		133	400	183	0.484	233	
34	P_4	84		134	143.6	184	25	234	
35		85	P_{45}	135	0.484	185	1500	235	
36		86		136	25	186	2142	236	
37	P_5	87		137	1500	187	0484	237	
38		88	P_{52}	138	10464	188	36	238	
39		89		139	0.484	189	400	239	
40	P_6	90		140	36	190	65.2	240	
41		91	P_{54}	141	400	191	0.484	241	
42		92		142	101.2	192	25	242	
43	P_8	93		143	0.484	193		243	
44		94		144	25	194		244	
45	P_9	95		145	1500	195		245	
46		96		146	14215	196		246	
47		97		147	0.484	197		247	
48		98		148	36	198			
49		99		149	400	199	5x10⁸		

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Step	User action	Display X	Y	Z
11	Press: CONTINUE.	2	2	2
	. Steps 3 to 10 are repeated for			
	. the second and subsequent			
	. circuit blocks until all 18			
	. circuit block data are entered.			
12	Press: CONTINUE.	2	2	0
13	Enter: Total number of output functions to be computed, 1, into X-register.	1		
14	Press: CONTINUE.	1	1	1
15	Enter: Transducer power gain code, 3, into Y-register. Plotted output (frequency response) code, 4, in X-register.	4	3	
16	Press: CONTINUE.	2	2	1
17a	Enter: X_o= 5x10^9 Hz into Y-register, X_{scale} = 2x10^8 Hz into X-register.	2x10^8	5x10^9	
17b	Press: CONTINUE.	2	2	2
17c	Enter: Y_o= 0, into Y-register, X_{scale}= 10db/inch, into X-register.	10	0	
17d	Press: CONTINUE.	3	3	0
20	Enter: Source resistance, R_s= 50 ohms into Y-register. Load resistance, R_L= 50 ohms into X-register.	50	50	
21	Press: CONTINUE.	4	4	0
22	Enter: f_H= 6.9x10^9 Hz into Z-register. f_1= 5.2x10^9 Hz into Y-register. Δf= 25x10^6 Hz omtp X-register.	25x10^6	5.2x10^9	6.9x10^9
23	Press: CONTINUE.	1	6	6
24	Press: CONTINUE.			

The input procedures are completed, and circuit analysis is automatically initiated.

A memory map for this circuit is shown in Fig. 3.9 to show the locations of the circuit data and sub-program storage location.

The frequency response of the filter is shown in Fig. 3.10. The in-band insertion loss has been re-plotted on the same figure using an expanded Y-scale. Experimental data are also superimposed on the same graph. They compare very favorably with the calculator prediction.

3.4.2 A 7 - 8 GHz microwave amplifier

This example illustrates the power of the program in the ability to accept matrix input. The transistor is described by scattering parameters, and the circuit is a combination of lumped and distributed parameter components.

The input of scattering parameters is accomplished by the use of special sub-routine, P7. Additional sub-programs to perform interpolation and convertion to chain matrix are devised (P33, P92 - P95). The operation details are described in Appendix III.

Shown in Fig. 3.11 is the circuit with the component values given in the accompanying table. Though the circuit execution details will not be presented as in the first example, a memory map is provided to indicate the element data storage locations. See Fig. 3.12 for the memory map.

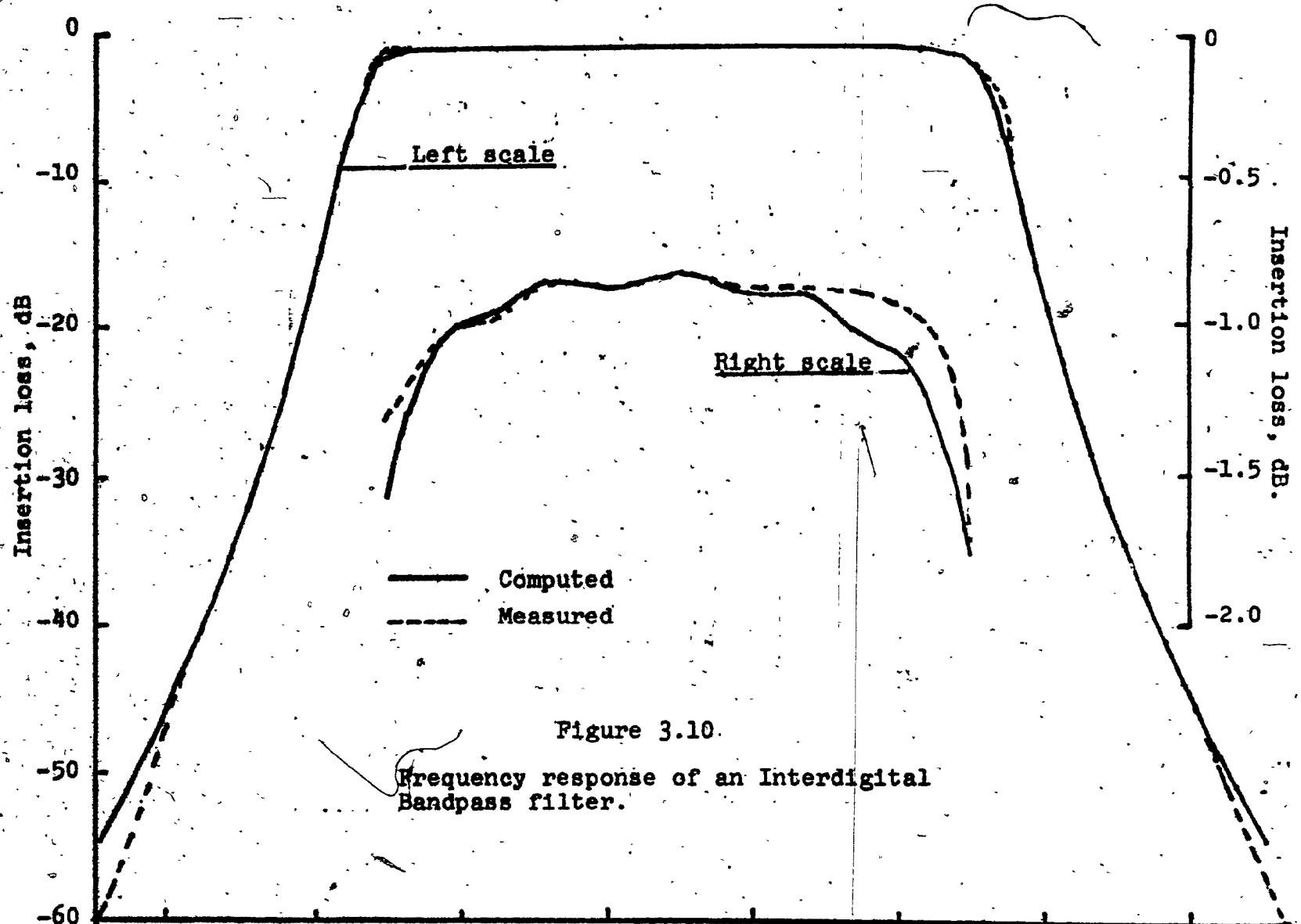
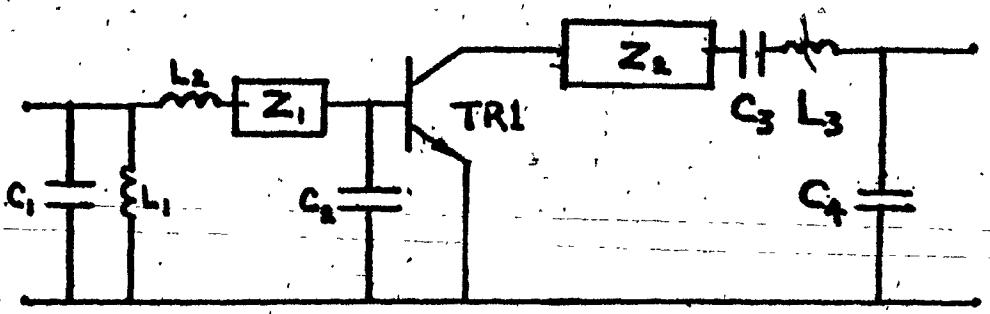


Figure 3.10.

Frequency response of an Interdigital Bandpass filter.



		S_{11}	S_{12}	S_{21}	S_{22}
S-paramener entry, Transistor type: H/P 35876.	7 GHz	0.524 ∠36°	0.145 ∠45°	1.04 ∠	0.66 ∠
	8 GHz	0.524 ∠	0.145 ∠	0.8 ∠	0.71 ∠

Element	Description
C_1	2×10^{-12} farad.
C_2	0.45×10^{-12} "
C_3	0.07×10^{-12} "
C_4	0.24×10^{-12} "
L_1	0.26×10^{-9} henry.
L_2	1.2×10^{-9} "
L_3	7.0×10^{-9} "
Z_1	50-ohm transmission line, 0.1 at 7.4 GHz.
Z_2	18-ohm transmission line, 0.286 at 6.4 GHz.

Figure 3.11

Circuit diagram of a 7 - 8 GHz amplifier

Title Memory map of the 7 - 8 GHz Amplifier. Date Feb. 1975 Page 1 of 1

Name C. H. C. L1

Figure 3.12

9101A MEMORY MAP

53

0		50		100		150	0.165	200	2×10^{6}
1		51	P7	101		151	75	201	0
2		52		102	P43	152	0.524	202	2
3	P1	53		103		153	-151	203	
4		54		104		154	0.66	204	
5		55	P33	105		155	-40	205	50
6		56		106		156	1.0	206	50
7		57	S-PARAMETER	107	P51	157	13	207	
8		58	CIRCUIT	108		158	0.146	208	
9		59	BLOCK	109		159	90	209	8
10		60		110	P54	160	0.524	210	
11		61		111		161	0.24×10^{12}	211	
12		62		112		162	1	212	
13		63	P95	113		163	0	213	
14		64		114		164	23	214	
15		65		115		165	0.07×10^{12}	215	
16		66		116	P42	166	7×10^{9}	216	
17	P2	67	P94	117		167	0	217	
18		68		118		168	12	218	
19		69		119		169	1000	219	
20		70		120		170	18	220	
21		71		121		171	0.525	221	
22		72		122		172	36	222	
23		73		123		173	50	223	
24		74		124	P36	174	8×10^{9}	224	
25		75		125		175	7×10^{9}	225	
26		76		126		176	33	226	
27		77		127		177	0.46×10^{12}	227	
28	P3	78		128		178	1	228	
29		79		129		179	0	229	
30		80		130		180	23	230	
31		81		131		181	1000	231	
32		82	P92	132	P12	182	50	232	
33		83		133		183	0.159	233	
34	P4	84		134		184	36	234	
35		85		135		185	1	235	
36		86		136		186	1.2×10^{9}	236	
37	P5	87	P93	137		187	0	237	
38		88		138	P23	188	12	238	
39		89		139		189	2×10^{12}	239	
40	P6	90		140		190	0.26×10^{9}	240	
41		91		141		191	0	241	
42		92		142		192	23	242	
43	P8	93		143		193	11	243	
44		94	P41	144		194	21	244	5×10^{5}
45	P9	95		145	-172	195	43	245	6.5×10^{8}
46		96		146	0.71	196	9	246	8.3×10^{9}
47		97		147	-50	197		247	
48		98		148	0.8	198			
49		99		149	1.0	199	6.4×10^{9}		

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The amplifier circuit is to be analysed for frequency response(transducer power gain), input and putput impedances in terms of reflection coefficients. The first output is to be plotted on linear frequency scale while the second and the third are presented as Smith Chart plots. In each instance experimental measurements are superimposed to show the close agreement between the calculator prediction and the experimental results. Fig. 3.13, 3.14, 3.15 show the three responses respectively.

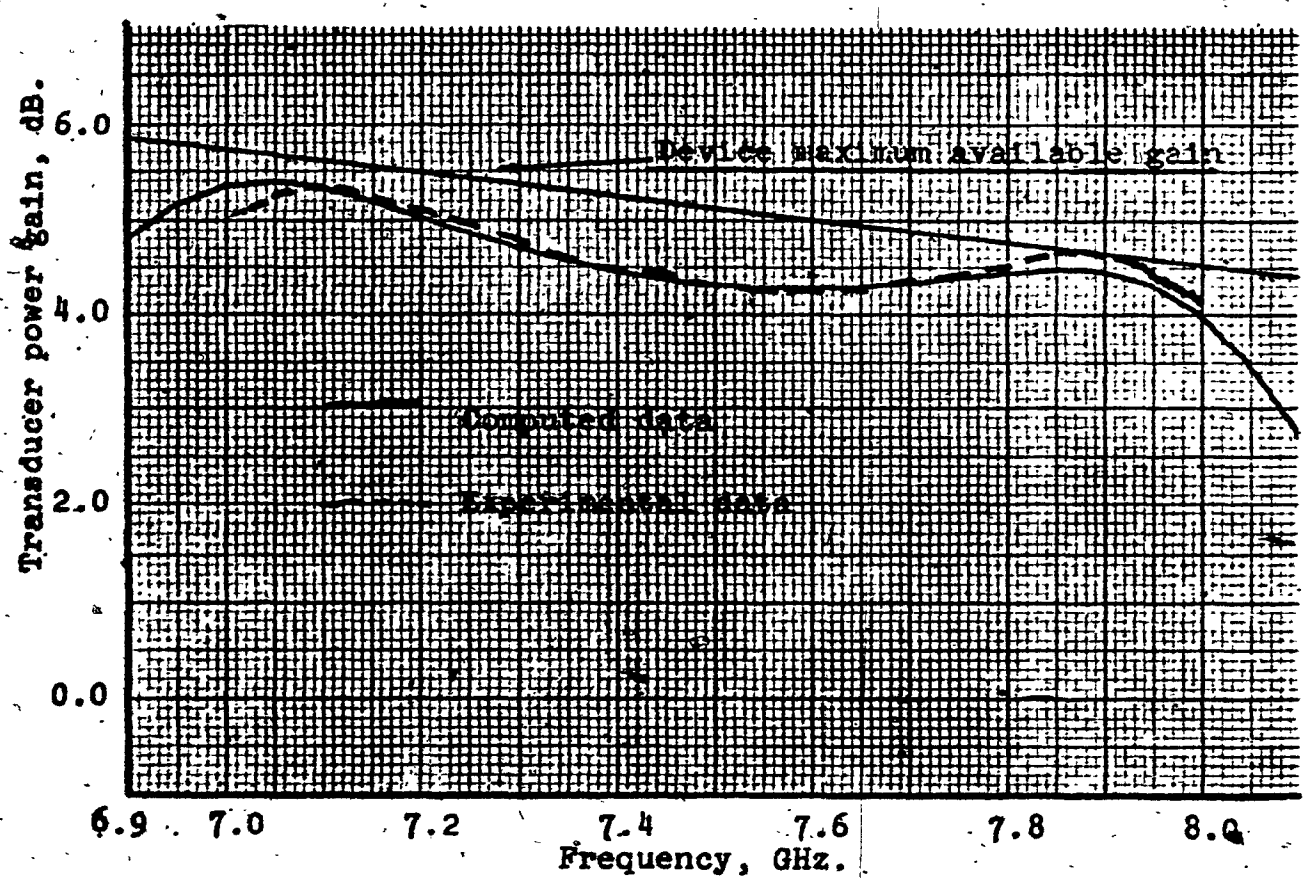


Figure 3.13

Frequency response of a 7 - 8 GHz Amplifier.

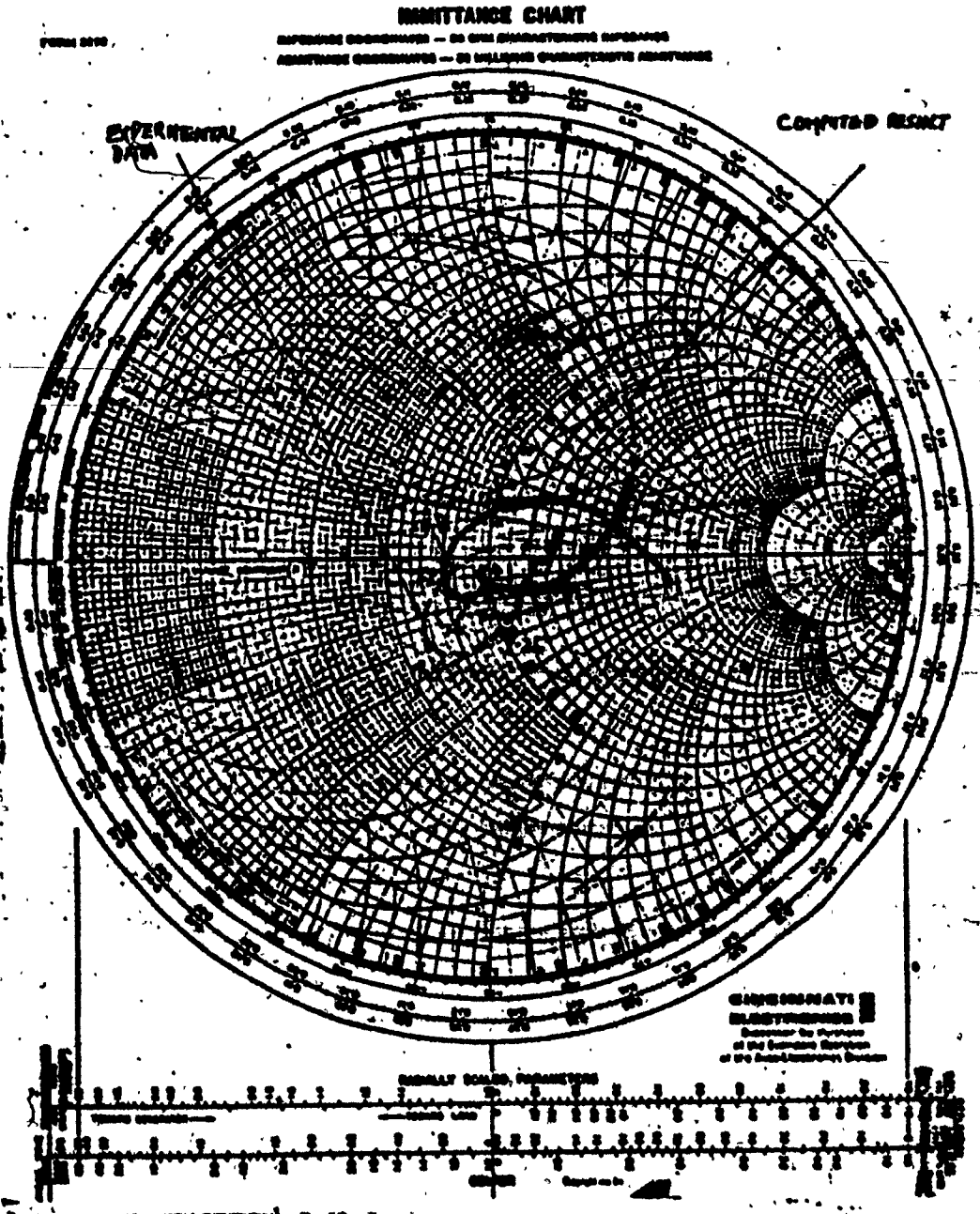


Figure 3.14

Smith Chart display of the input impedance of a 7 - 8 GHz

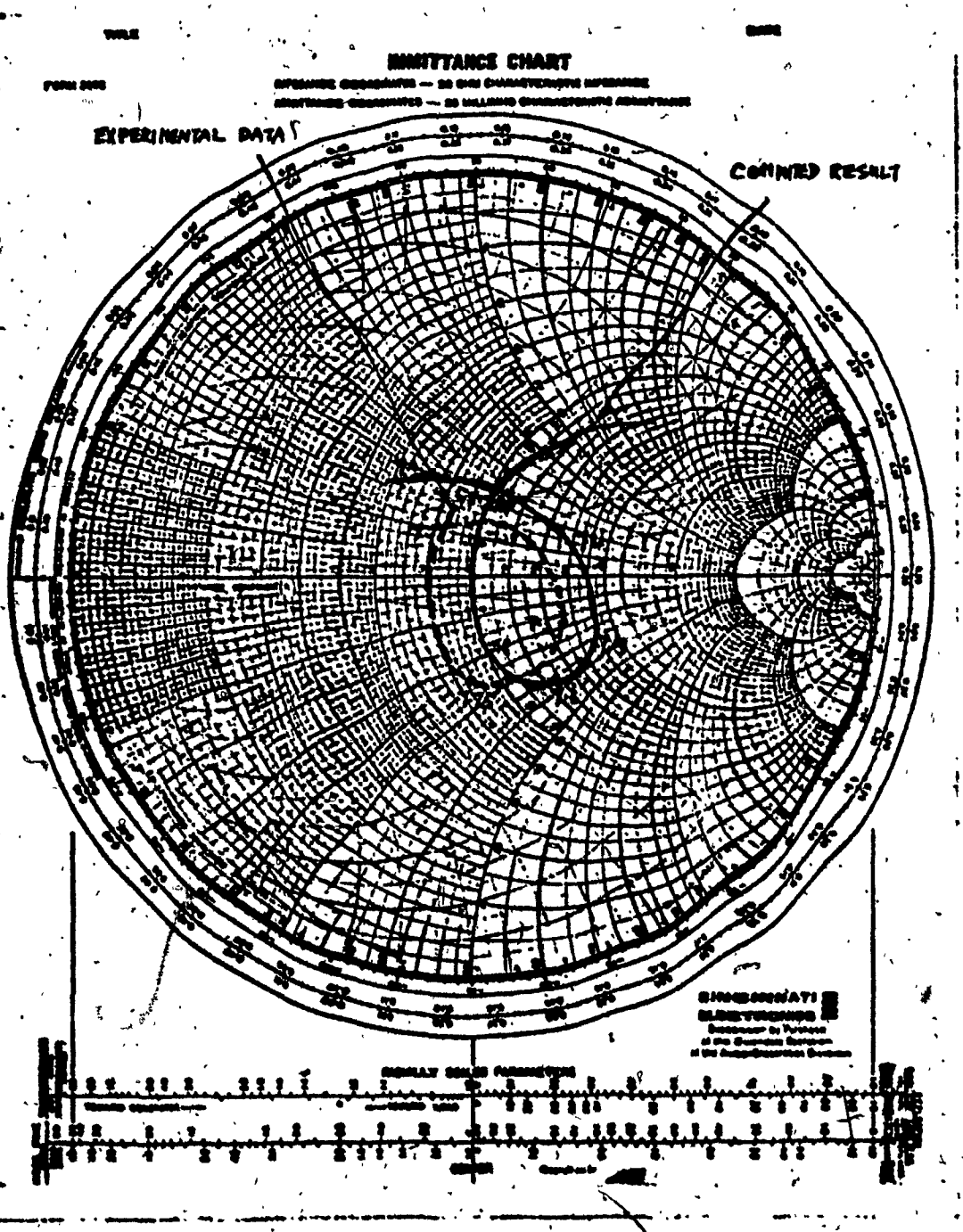


Figure 3.15

Smith Chart display of the output impedance of a 7 - 8 GHz amplifier.

CHAPTER 4

TIME DOMAIN CIRCUIT ANALYSIS PROGRAM

4.1 Program development

This program is designed to have a similar general structure as the Frequency Domain Circuit Analysis Program. The overall program consists of five main bodies:

- Input sub-program to accept circuit data.
- Circuit analysis sub-program.
- Output function formation sub-program.
- Output time function computation sub-program to obtain the response r(t) for a given exciation e(t).
- Output presentation sub-program.

Due to the unique properties of time domain analysis, the circuit analysis approach is not identical in numerical technique as in the frequency domain analysis. It is to be pointed out though that the basic approach of chain matrix multiplication is still the fundamental basis behind the analysis.

Following the discussion of section 2.4, the

general philosophy of time domain circuit analysis is:

- Formation of a complex variable system function, $H(S) = N(S)/D(S)$.
- Solution of the response function for the system function H(S) with a given excitation. This in effect, is the problem of solving an inhomogeneous linear differential equation with the forcing function e(t).

Due to the size of the overall program, it is not possible to store all the sub-programs at the same time in the available memory space in the extended memory unit. The overall programming structure of 5 main bodies are re-grouped into 4 sub-programs including the input sub-program. This input sub-program, similar to that used in the Frequency Domain Circuit Analysis Program, is not to be stored into the extended memory. The remaining 3 are: circuit analysis sub-program, system function formation sub-program, and the response time function computation sub-program. The overall system is shown in the simplified flow-chart of Fig. 4.1.

As a result of the numerical technique employed in the output function solution, there is one major difference in performance between this program and the Frequency Domain Analysis Program. In the present case, the accuracy of the output time function is dependent on the size of the

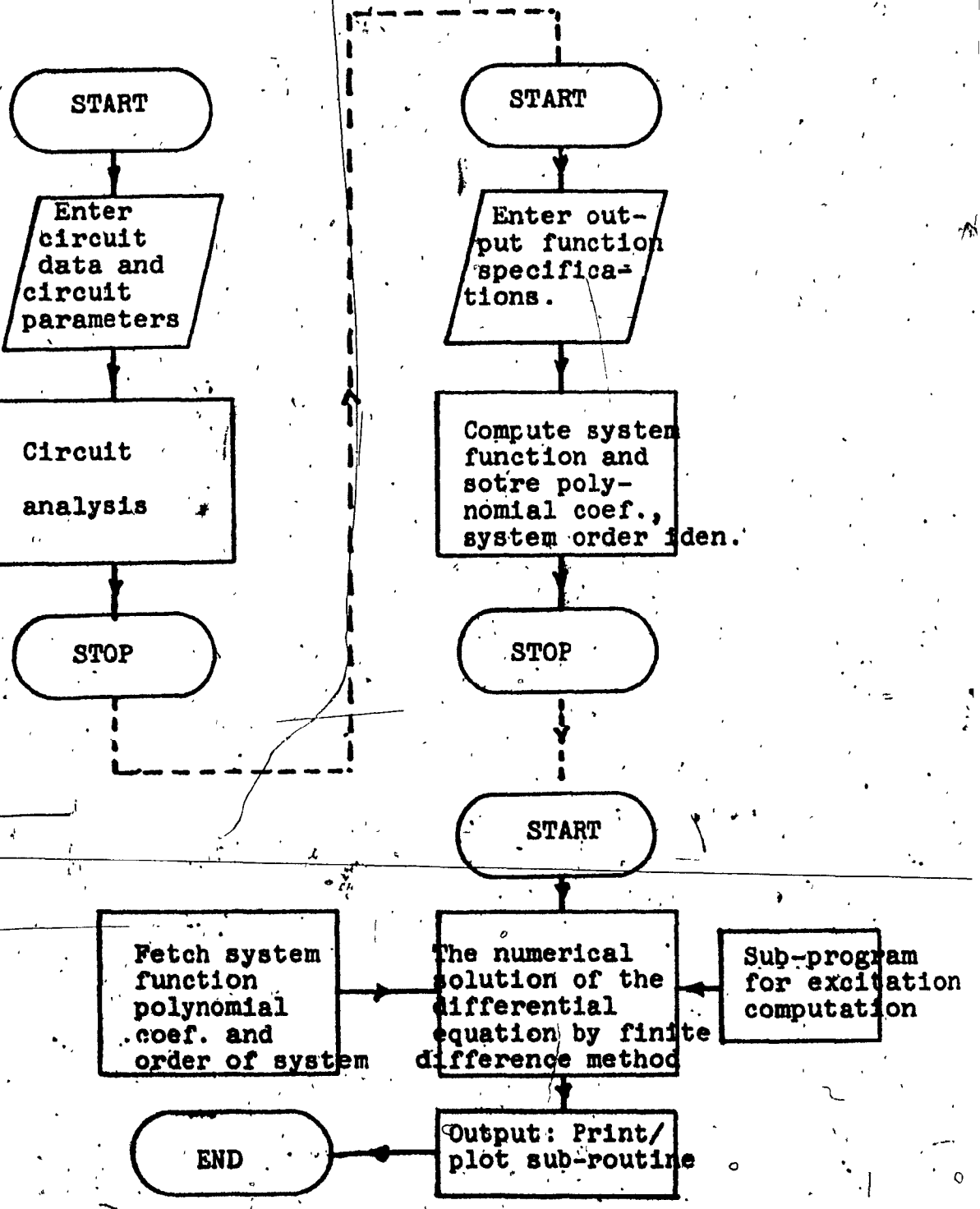


Figure 4.1

Simplified overall flow-chart of the Time Domain Circuit Analysis Program

sampling interval - the smaller it is, the more accurate is the result. Nevertheless, due to the very nature of numerical analysis, the result will never be exact though a very good accuracy can be achieved by using sufficiently small sampling interval.

4.1.1 Input and circuit analysis sub-programs

Since the input sub-program is designed to be similar to that used in the Frequency Domain Analysis Program, the discussion here will only emphasize the difference.

Using identical circuit coding system, the program accepts the description of the circuit blocks as shown in Table 3.1. The exception is that the circuit types are restricted to R-L-C lumped elements, corresponding to polynomial functions. The complexity of the circuit is restricted to analysing a maximum of 9 independent energy storage elements (9^{th} order system). Furthermore, only one system function can be computed at a time. The total input sequence is summarized below:

Step	Description
1	Enter N, the total number of circuit blocks contained in the overall network.
2	Describe the circuit blocks by connection codes and circuit component codes (similar to that of the Frequency Domain Analysis Program).
3	Specify the required system function.
4	Specify the source and load resistances.

The acceptable input circuit blocks and output functions are summarized in Table 4.1.

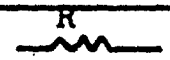
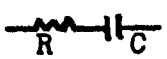
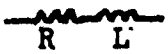
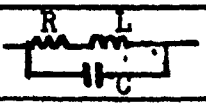
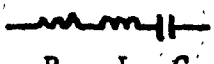
Circuit analysis is performed using matrix multiplication technique. Polynomial functioned matrix multiplication is the theme of the circuit analysis program. It is achieved through the development of several sub-routines to perform polynomial multiplication, addition, and cancellation of common factor in S between the nimerator and the denominator. The importance of the third property cannot be ignored. Consider a simple algebraic expression:

$$\frac{A}{S} + \frac{B}{S}$$

The answer is obviously (A + B)/S by inspection. But if the expression is to be evaluated by the sub-programs which will

Circuit connection code (P)

"Series" 1
"Shunt" 2

Circuit type	Description	Code (Q)	Data entry sequence at X-register display of 1	2	3
	Resistor(Ohms)	1	R	0	0
	Series R-C (Ohms/farads)	2	R	0	C
	Series R-L (Ohms/henries)	3	R	L	0
	Parallel R-L-C (Ohms/henries/farads)	4	R	L	C
	Series R-L-C (Ohms/henries/farads)	5	R	L	C

(a) Acceptable Input Circuit Description

Output presentation code (Q)

Print 1
Plot 2

System Function	Code (P)	Definition
Input imdedance, Z_{in}	1	V_{in}/I_{in}, Output terminated by R_L.
Input admittance, Y_{in}	2	I_{in}/V_{in}, "
Voltage transfer function, A_v	3	V_{out}/V_{in}, "
Trans-impedance, Z_{21}	4	V_{out}/I_{in}, "

(b) Available system functions

TABLE 4.1

Acceptable input circuit blocks and output functions
(Time domain analysis)

perform cross multiplication, the result will be:

$$\frac{AS + BS}{S^2}$$

The effect is that the degrees of the polynomials are unnecessarily and harmfully raised, resulting in a drastic reduction of the capability of handling higher order systems. With the use of the "Common factor in 'S' cancellation sub-routine", this situation is avoided.

Sub-program P1 initiates the circuit analysis and sub-programs P2, 3, and 4 perform the necessary matrix multiplication. Sub-routines P90, 91, 92, 93, 94, and 95 provide the necessary tools for the polynomial function manupilations.

To simplify the computation of the system functions, the effects of the source and load are included in the overall circuit analysis. No loss of generality would result as R_S and R_L can be set to any values including 0 and infinity to suit the situation.

The flow-charts are shown in Fig. 4.2(a), (b), with the

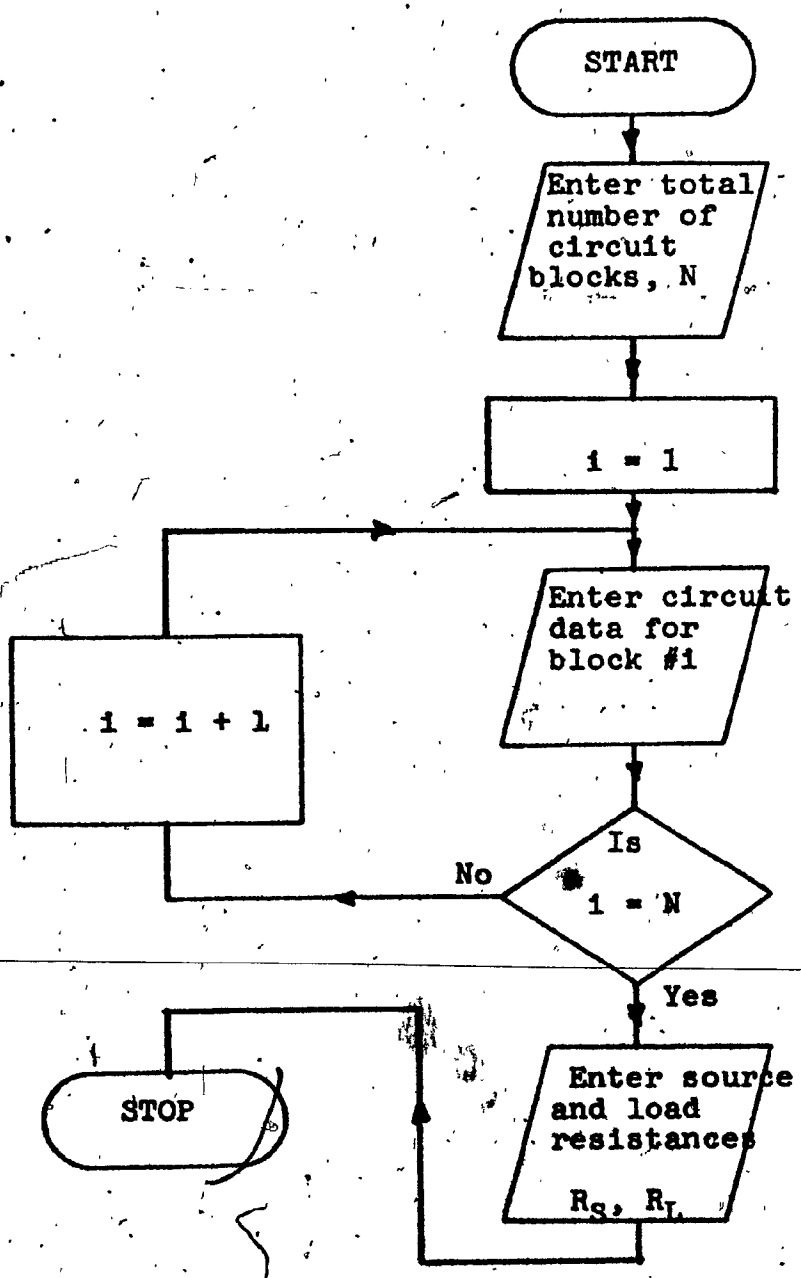


Figure 4.2 (a)

Flow-chart of the Input sub-program for Time Domain Circuit Analysis Program

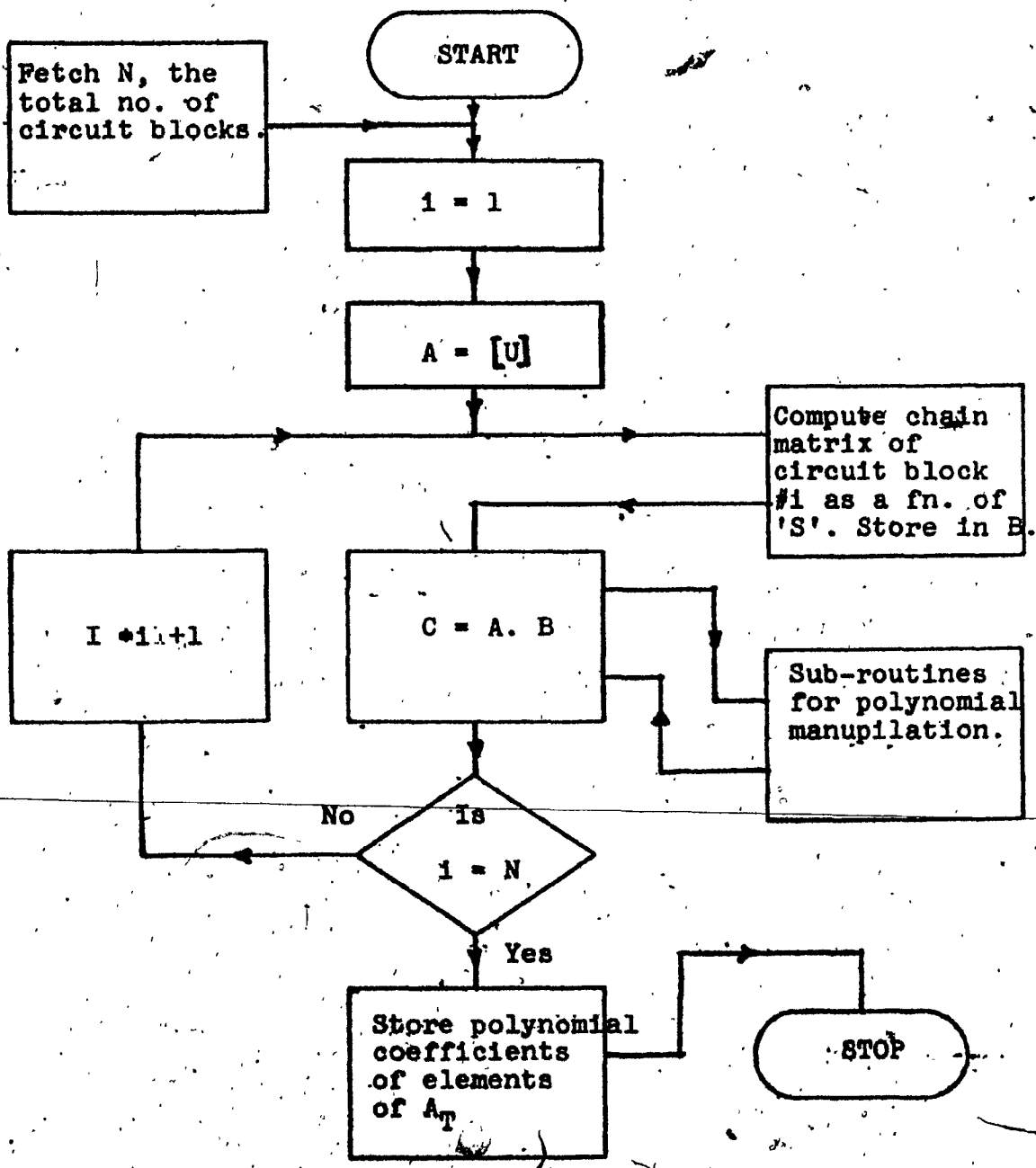


Figure 4.2 (b)

Flow-chart of the circuit analysis sub-program for Time Domain Circuit Analysis Program

memory map shown in Fig. 4.3.

4.1.2 System function formation sub-program

At he completion of the circuit analysis sub-program, the polynomial coefficients of the final chain matrix elements are stored for use in the formation of the specified system function. Instruction is also given as an input to this sub-program as to whether the final output time function is to be printed or plotted against time, t. When the plotter output is specified, additional information like the origin coordinates, the X and Y axes scaling factors are to be entered. Also to be specified in this sub-program are the size of the sampling interval and the maximum number of points the user wants to calculate, before the output function computation sub-program stops automatically.

Since the only interested circuit variables are V_{in}, I_{in}, V_{out}, I_{out}, 4 system function calculations are provided:

- $Z_{in} = V_{in}/I_{in}$ 4.1.1
- $Y_{in} = I_{in}/V_{in}$ 4.1.2
- $A_v = V_{out}/V_{in}$ 4.1.3
- $Z_{21} = V_{out}/I_{in}$ 4.1.4

Figure 4.3 # 9101A MEMORY MAP

0		50	P91:	100		150		200	
1		51	MATRIX DATA	101		151	a_{21}	201	TEMPORARY
2	P1:	52	TRANSFER	102		152	NUMERATOR	202	MEMORY
3		53		103	BLOCK #2	153	COEFFICIENTS	203	
4	CIRCUIT	54		104		154		204	
5	ANALYSIS	55	P92:	105		155		205	
6	INITIALIZATION	56	DEGREE DETEC-	106		156		206	
7		57	TION OF POLY.	107	BLOCK #1	157		207	
8		58	P93:	108		158		208	
9		59	POLYNOMIAL	109		159		209	
10		60	ADDITION	110	CHAINMATRIX	160		210	POLYNOMIAL
11		61	P94:	111	COEFFICIENTS:	161	a_{2i}	211	MANUPILATION
12	P2:	62	ELIMINATION OF	112		162	DENOMINATOR	212	TEMPORARY
13		63	COMMON FACTORS	113	a_{1i} NUMERATOR	163	COEFFICIENTS	213	MEMORY
14	POLYNOMIAL	64	IN S TW BOTH	114	COEFFICIENTS	164		214	SPACE
15	MATRIX	65	DENOMINATOR AND	115		165		215	
16	MULTIPLICATION	66	NUMERATOR OF	116		166		216	
17		67	POLYNOMIAL	117		167		217	A(S)
18	P3:	68	RATIO N(S)/D(S)	118		168		218	
19		69	P95:	119		169		219	
20	POLYNOMIAL	70	DETECTION OF	120		170		220	
21	FUNCTIONS	71	LOWERS DEGREE	121		171	a_{22}	221	
22	MANUPILATION	72	IN POLYNOMIAL	122		172	NUMERATOR	222	
23	FOR THE	73		123	a_{1i} DENOMINA-	173	COEFFICIENTS	223	
24	MATRIX ELEMENTS	74		124	TOR COEFFICIENTS	174		224	
25	COMPUTATION	75	P14:	125		175		225	B(S)
26		76	SERIES CONNECTED	126		176		226	
27		77	PARALLEL R-L-C	127		177		227	
28		78		128		178		228	
29		79	P15:	129		179		229	
30		80	SERIES CONNECTED	130		180		230	
31		81	SERIES R-L-C	131	a_{12}	181	a_{12}	231	
32		82		132	NUMERATOR	182	DENOMINATOR	232	
33	P4:	83	P24:	133	COEFFICIENTS	183	COEFFICIENTS	233	C(S)
34		84	SHUNT CONNECTED	134		184		234	
35	CONTINUATION	85	PARALLEL R-L-C	135		185		235	
36	OF P3.	86		136		186		236	
37		87	P25:	137		187		237	
38		88	SHUNT CONNECTED	138		188		238	
39	P8:	89	SERIES R-L-C	139		189		239	
40	UNITY MATRIX	90		140		190	TEMPORARY	240	WORK AREA
41	FORMATION	91		141	a_{12}	191	MEMORY	241	"
42		92		142	DENOMINATOR	192		242	"
43	P90:	93		143	COEFFICIENTS	193		243	"
44		94		144		194	CIRCUIT BLOCK	244	R5
45	POLYNOMIAL	95		145		195	CHAIN MATRIX	245	RL
46	MULTIPLICATION	96	CIRCUIT	146		196	FORMATION	246	K=BLOCK CONNECTION
47		97	BLOCK	147		197	NUMERATOR COE	247	N
48		98	INPUT	148		198	DENOMINATOR		
49		99	DATA	149		199	COEFFICIENTS		

The sub-programs prepared for the above functions are for the circuit driven and terminated by the specified R_S and R_L. When needed, user-defined functions can be programmed and incorporated.

The flow-chart and its memory map are shown in Fig. 4.4 and Fig. 4.5 respectively.

4.1.3 Response time function computation sub-program

The fundamental principle used in this sub-program has been outlined in the mathematical treatment in section 2.4. Using equation 2.4.7, the output time function r(KT) is computed numerically for the given excitation e(KT).

A special feature of this program is the ability to accept the user-defined excitation function. The excitation will be programmed and the sub-program is designated P10. While this excitation is, in general, a function expressed by mathematical equations, it is also possible to be in a table form.

The computed output is presented in sub-routine P11 which may represent a printer output or plotter output as required by the user. Built in to the present system, P11

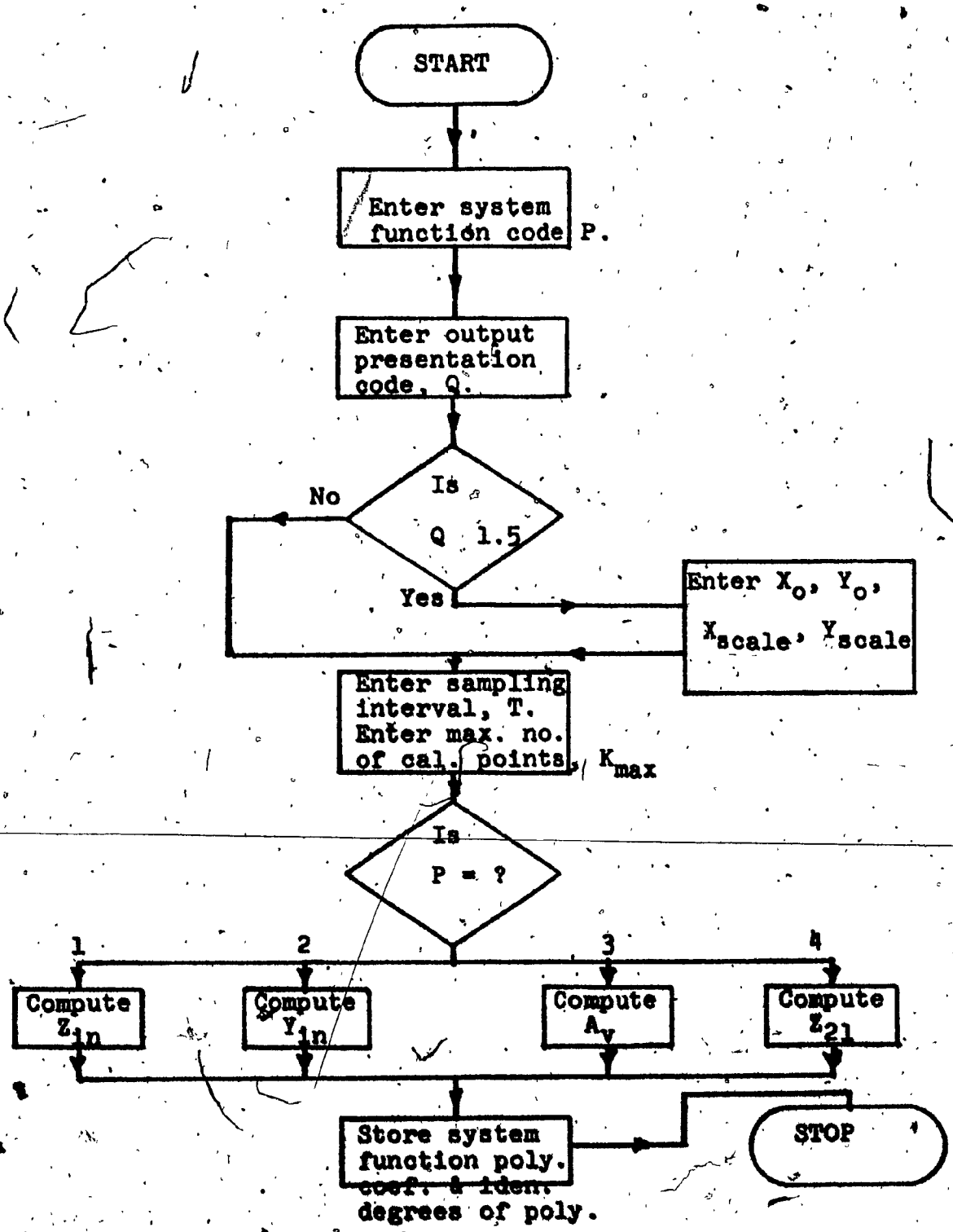


Figure 4.4

Flow-chart of System Function Formation Sub-program

Figure 4.5 9101A MEMORY MAP

0	P5:	50	P91:	100		150		200	DENOMINATOR b_0
1		51	MATRIX DATA	101		151	FINAL CHAIN	201	COEFFICIENT b_1
2	SYSTEM FUNCTION	52	TRANSFER	102		152	MATRIX POLY-	202	b_2
3	SPECIFICATION	53		103		153	NOMIALS	203	b_3
4	PROGRAM	54		104		154	COEFFICIENT	204	b_4
5		55	P92:	105	PRINT/PLOT CODE	155	STORAGE	205	b_5
6		56	DEGREE DETECTION	106	DATA X_0	156		206	b_6
7		57	OF POLYNOMIAL.	107	FOR ΔX/INCH	157		207	b_7
8		58	P93:	108	PLOTTER Y_0	158		208	b_8
9		59	POLYNOMIAL	109	ΔY/INCH	159		209	b_9
10	P81:	60	ADDITION	110		160		210	POLYNOMIAL
11		61	P94:	111		161		211	MANUPULATION
12	INPUT IMPEDANCE	62	CANCELLATION	112		162		212	WORK
13	FUNCTION	63	OF COMMON	113		163		213	AREA
14		64	FACTOR IN S	114		164		214	
15	$Z_{IN} = \frac{V_{IN}}{I_{IN}}$	65	IN BOTH DENOMI-	115		165		215	
16		66	NATOR AN NUME-	116		166		216	A(S)
17		67	RATOR OF POLY.	117		167		217	
18		68	FUNCTION N/M.	118		168		218	
19		69	P95:	119		169		219	
20	P82:	70	DETECTION OF	120		170		220	
21		71	LOWEST DEGREE	121		171		221	
22	OUTPUT IMPEDANCE	72	IN POLYNOMIAL	122		172		222	
23	FUNCTION	73		123		173		223	
24		74		124		174		224	B(S)
25	$Z_{OUT} = \frac{V_{OUT}}{I_{OUT}}$	75		125		175		225	
26		76		126		176		226	
27		77		127		177		227	
28		78		128		178		228	
29		79		129		179		229	
30	P83:	80		130		180		230	
31	VOLTAGE TRAN-	81		131		181		231	
32	SFER FUNCTION	82		132		182		232	
33	P84:	83		133		183		233	C(S)
34	TRANS-IMPEDANCE	84		134		184		234	
35	Z_{21}.	85		135		185		235	
36		86		136		186		236	
37		87		137		187		237	
38		88		138		188		238	
39		89		139		189		239	
40		90		140		190	a_0	240	OUTPUT FL. CODE
41		91		141		191	a_1	241	
42	P90	92		142		192	SYSTEM a_2	242	
43		93		143		193	FUNCTION a_3	243	M
44	POLYNOMIAL	94		144		194	a_4	244	N
45	MULTIPLICATION	95		145		195	NUMERATOR a_5	245	KMAX
46		96		146		196	COEFFICIENT a_6	246	K
47		97		147		197	a_7	247	T
48		98		148		198	a_8		
49		99		149		189	a_9		

represents a plotting sub-routine that plots both the input excitation and output response versus time.

The flow-chart is shown in Fig. 4.6 with the memory map shown in Fig. 4.7.

4.2 Program loading

As discussed in section 4.1, the time domain circuit analysis program consists of three independent systems:

- Input and circuit analysis sub-programs.

  P0 is responsible for data entry. It is not to be stored in the extended memory.
  P1, 2, 3, 4, 8, 90, 91, 92, 93, 94, and 95 perform circuit analysis (matrix multiplication).
  P14, 15, 24, 25 (also P11, 12, 13, 21, 22, 23) supply the circuit component chain matrices.
- System function formation sub-programs.

  P5 initiates the function formation and accepts other system information for computation.
  P81, 82, 83, and 84 supply the desired system function formation.

- Response time function computation sub-programs.

  P2, 3, 4, 5, 7, and 8 computes the output function.
  P10 defines the input excitation.
  P11 is the output presentation sub-routine.
  P6 evaluates X!, to be used in the output function computation.

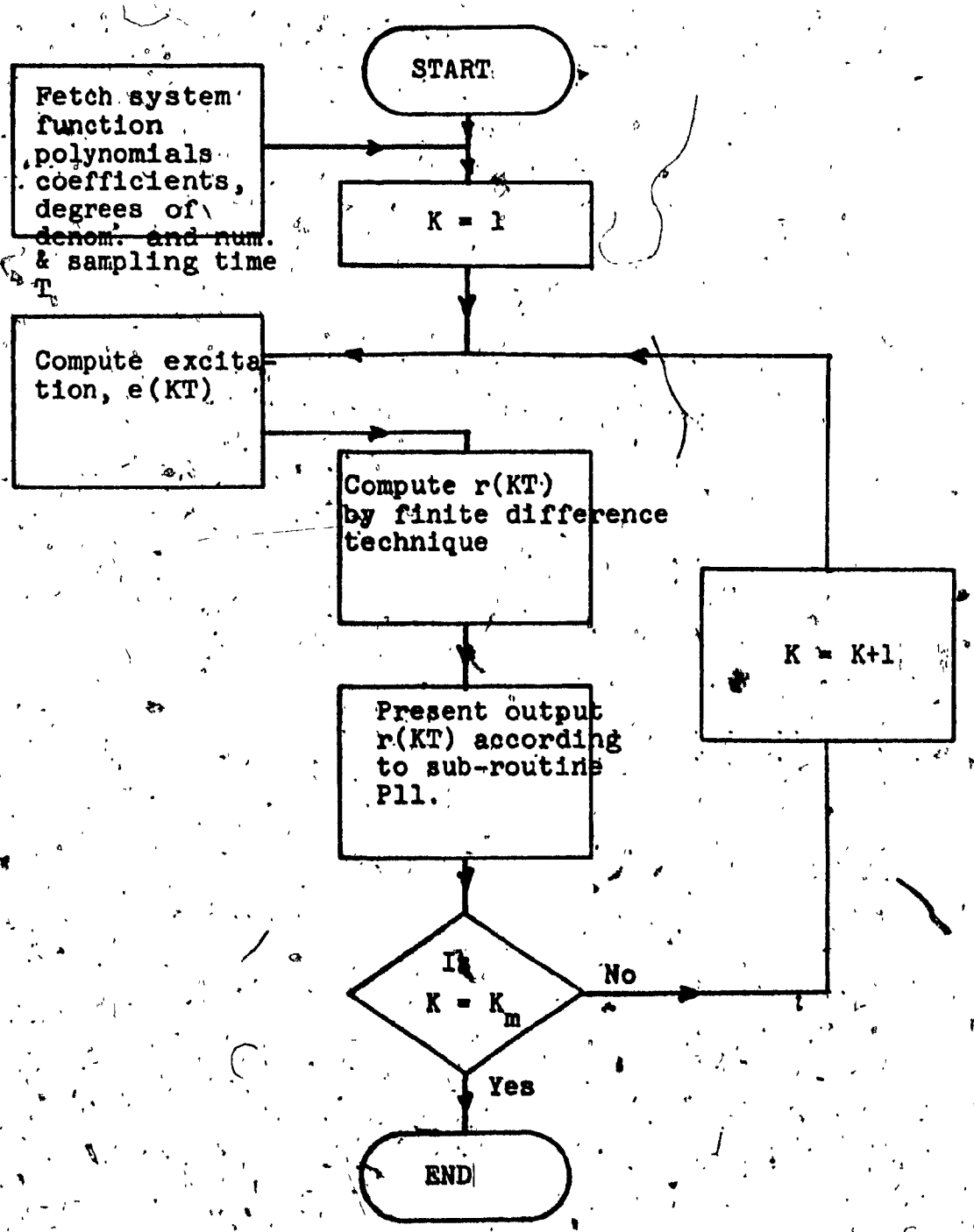


Figure 4.6

Flow-chart of the response function computation sub-program

Figure 4.7 9101A MEMORY MAP

0		50	SAMPLE INPUT	100		150	FINAL CHAIN	200	DENOMINATOR b_0
1	P2:	51	EXCITATION (U(t))	101		151	MATRIX POLY-	201	COEFFICIENTS b_1
2	RESPONSE	52	P11:	102		152	NOMIALS	202	b_2
3	TIME FUNCTION	53	PLOT SUB-	103		153	COEFFICIENT	203	b_3
4	COMPUTATION	54	ROUTINE.	104		154	STORAGE	204	b_4
5	INITIALIZATION	55	(SHOW INPUT	105		155		205	b_5
6		56	AND OUTPUT	106	DATA X_0	156		206	b_6
7		57	SIMULTANEOUSLY)	107	FOR ΔX/in.	157		207	b_7
8	P3:	58		108	PLOTTER Y_0	158		208	b_8
9		59		109	ΔY/in.	159		209	b_9
10	FINAL CALCU-	60		110		160		210	$e(K-9)T$
11	LATION OF	61		111		161		211	INPUT $e(K-8)T$
12	RESPONSE TIME	62		112		162		212	EXCITATION $e(K-7)T$
13	FUNCTION, T(t)	63		113		163		213	$e(K-6)T$
14		64		114		164		214	$e(K-5)T$
15		65		115		165		215	$e(K-4)T$
16	P4:	66		116		166		216	$e(K-3)T$
17	COMPUTE	67		117		167		217	$e(K-2)T$
18	$\sum \frac{a_n}{T^n}$	68		118		168		218	$e(K-1)T$
19		69		119		169		219	$e(KT)$
20	P5:	70		120		170		220	RESPONSE $r(K-9)T$
21		71		121		171		221	FUNCTION $r(K-8)T$
22	COMPUTE	72		122		172		222	$r(K-7)T$
23		73		123		173		223	$r(K-6)T$
24	$\sum_{j=1}^{n} \frac{g(K-j)(-1)^j}{(n-j)!\,j!}$	74		124		174		224	$r(K-5)T$
25		75		125		175		225	$r(K-4)T$
26		76		126		176		226	$r(K-3)T$
27		77		127		177		227	$r(K-2)T$
28		78		128		178		228	$r(K-1)T$
29		79		129		179		229	$r(KT)$
30		80		130		180		230	$T(KT)$
31	P6:	81		131		181		231	
32		82		132		182		232	WORK AREA
33	COMPUTE X!	83		133		183		233	FOR INDEX
34		84		134		184		234	BOOK-KEEPING
35	P7:	85		135		185		235	
36	COMPUTE	86		136		186		236	
37	$\sum_{n=1}^{N} \frac{a_n n!}{T^n}$	87		137		187		237	
38		88		138		188		238	
39		89		139		189		239	
40	$\sum_{j=1}^{n} \frac{a(K-j)T(-1)^j}{(n-j)!\,j!}$	90		140		190	a_0	240	
41		91		141		191	a_1	241	
42		92		142		192	SYSTEM a_2	242	
43		93		143		193	FUNCTION: a_3	243	M
44		94		144		194	a_4	244	N
45	P8:	95		145		195	NUMERATOR a_5	245	K_{MAX}
46	$e(K-1)T = e(KT)$	96		146		196	COEFFICIENTS a_6	246	K
47	$r(K-1)T = r(KT)$	97		147		197	a_7	247	T
48	FOR ALL K	98		148		198	a_8		
49	P10:	99		149		199	a_9		

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The details of the program loading procedures for each sub-program system are given below:

. Circuit analysis sub-program

File protect switch (Extended memory unit): OFF.

Step	User action	Display X	Y	Z
1	Press: CLEAR, FMT, SET FLAG.	0	0	0
2	Enter: P1.			
3	Press: 1, FMT, FMT.	11	0	0
4	Enter: P2.			
5	Press: 2, FMT, FMT.	17	0	0
6	Enter: P3.			
7	Press: 3, FMT, FMT.	31	0	0
8	Enter: P4.			
9	Press: 4, FMT, FMT.	38	0	0
10	Enter: P8.			
11	Press: 8, FMT, FMT.	41	0	0
12	Enter: P90.			
13	Press: 90, FMT, FMT.	49	0	0
14	Enter: P91.			
15	Press: 91, FMT, FMT.	54	0	0
16	Enter: P92.			
17	Press: 92, FMT, FMT.	57	0	0
18	Enter: P93.			
19	Press: 93, FMT, FMT.	60	0	0
20	Enter: P94.			
21	Press: 94, FMT, FMT.	68	0	0
22	Enter: P95.			
23	Press: 95, FMT, FMT.	74	0	0
24	Enter: P14.			
25	Press: 14, FMT, FMT.	78	0	0
26	Enter: P15.			
27	Press: 15, FMT, FMT.	82	0	0
28	Enter: P24.			
29	Press: 24, FMT, FMT.	86	0	0
30	Enter: P25.			
31	Press: 25, FMT, FMT.	90	0	0
32	Press: END.			
33	Enter: P0.			
34	File protect switch (Extended memory unit): ON.			

After the execution of the circuit analysis sub-program, the system function formation sub-program is to be loaded as follows:

. System function formation sub-program

File protect switch (Extended memory unit): OFF

Step	User action	Display X	Y	Z
1	Press: CLEAR, FMT, SET FLAG.	0	0	0
2	Enter: P5.			
3	Press: 5, FMT, FMT.	9	0	0
4	Enter: P81.			
5	Press: 81, FMT, FMT.	19	0	0
6	Enter: P82.			
7	Press: 82, FMT, FMT.	29	0	0
8	Enter: P83.			
9	Press: 83, FMT, FMT.	32	0	0
10	Enter: P84.			
11	Press: 84, FMT, FMT.	35	0	0
12	File protect switch (Extended memory unit): ON.			

After the execution of the system function formation sub-program, the output response function computation program is to be loaded as follows:

. Response time function computation sub-program

File protect switch (Extended memory unit): OFF

Step	User action	Display X	Y	Z
1	Program the excitation time function and designate it as P10. Record on a magnetic card.			
2	Program or select the output presentation sub-routine and designate it as P11. Record (if required) on a magnetic card.			
3	Press: CLEAR, FMT, SET FLAG.	0		
4	Enter: P2.			
5	Press: 2, FMT, FMT.	7		
6	Enter: P3.			
7	Press: 3, FMT, FMT.	15		
8	Enter: P4.			
9	Press: 4, FMT, FMT.	19		
10	Enter: P5.			
11	Press: 5, FMT, FMT.	30		
12	Enter: P6.			
13	Press: 6, FMT, FMT.	34		
14	Enter: P7.			
15	Press: 7, FMT, FMT.	40		
16	Enter: P8.			
17	Press: 8, FMT, FMT.	44		
18	Enter: P10.			
19	Press: 10, FMT, FMT.			
20	Enter: P11.			
21	Press: 11, FMT, FMT.			
22	File protect switch (Extended memory unit): ON.			

All the program loading steps are completed and the sub-program is ready for execution.

4.3 Program execution

The overall program execution consists of successively executing the three sub-program bodies loaded individually as described in the procedures of section 4.2.

. Input and circuit analysis sub-programs

PROGRAM/RUN switch: RUN.

(The following steps are to be executed after the input and circuit analysis sub-programs are loaded according to the procedures in section 4.2)

Step	User action	Display X	Y	Z
1	Press: END, CONTINUE.	1	1	0
2	Enter: Total number of circuit blocks, N, in X-register.			
3	Press: CONTINUE. where "i" indicates that the data for block #i are to be entered. i = 1, 2, ...N.	i	i	i
4	Enter: Circuit connection code, P, in X-register, and circuit type code, Q, in Y-register. This is for circuit block #i. (Refer to table 4.1 for P, Q.)	P	Q	
5	Press: CONTINUE. "1" in X-register display indicates first element value of circuit block #i is to be entered. Y-register display indicates subroutine P'PQ' is to be used to form the chain matrix for that circuit block.	1	PQ	i
6	Enter: First element value of circuit block #i in X-register.	a_1		
7	Press: CONTINUE.	2	PQ	i
8	Enter: Second element value for circuit block #i in X-register.	a_2		
9	Press: CONTINUE.	3	PQ	i
10	Enter: Third element value for circuit block #i in X-register.	a_3		
11	Press: CONTINUE.	i+1	i+1	i+1
	Steps 3 to 10 are repeated for data entry to the #(i+1) circuit block. This process is repeated until the circuit informations of all N circuit blocks are entered.			
12	Press: CONTINUE.	2	2	0
13	Enter: Source and load resistances, R_S - Y-register, R_L - X-register.	R_L	R_S	

Step	User action	Display X	Y	Z
14	Press: CONTINUE.			
15	Press: END, 1, FMT, GO TO.	11		
16	Press: END, CONTINUE.			

The circuit analysis sub-program is initiated by step 16. The calculator registers will periodically flash-display the circuit block number "i" to indicate that circuit block #i is currently being analysed.

Next to be executed after the circuit analysis sub-program is the system function formation sub-program. This sub-program is to be loaded according to the description in section 4.2 after the complete execution of the circuit analysis sub-program. The execution sequence is given below:

System function formation sub-programs

PROGRAM/RUN switch: RUN.

Step	User action	Display X	Y	Z
1	Press: 5, FMT, GO TO.	9		
2	Press: END, CONTINUE.	3	3	0
3	Enter: System function code, P, in X-register. (See table 4.1 for P.)	P		
4	Press: CONTINUE.	4	4	0
5	Enter: Print/Plot decision code, Q, in X-register. Print = 1, Plot = 2.	Q		
6	Press: CONTINUE. (If Q = 1, go to step 8.) (If Q = 2, continue.)	5 4	5 4	0 1
7a	Enter: X coordinate of origin into Y-register, X axis scale factor in units/inch, into X-register.	X_{scale}	X_o	

Step	User action	Display X	Y	Z
7b	Press: CONTINUE.	4	4	0
7c	Enter: Y coordinate of origin into Y-register, Y axis scale factor in units/inch, into X-register.	Y_{scale}	Y_o	
7d	Press: CONTINUE.	5	5	
8	Enter: Sampling interval, T, into X-register: Maximum number of points to be computed K_{max}, into Y-register.	T	K_{max}	
9	Press: CONTINUE.			

The system function formation sub-programs are automatically initiated after the completion of data entry. The program will stop when the execution is completed with the results stored for use in the output function computation.

The output response time function computation sub-programs are loaded next according to the procedures in section 4,2. The keyboard entry:

	X-register display
CLEAR, 2, FMT, GO TO.	7
END, CONTINUE	

will initiate the computation process. At the conclusion of the analysis, the result will be presented by the printer or plotter as specified.

4.4 Circuit analysis examples

Two examples, a low-pass filter output for a pulse excitation, and a step response of a second order bandpass structure, are presented to illustrate the program performance.

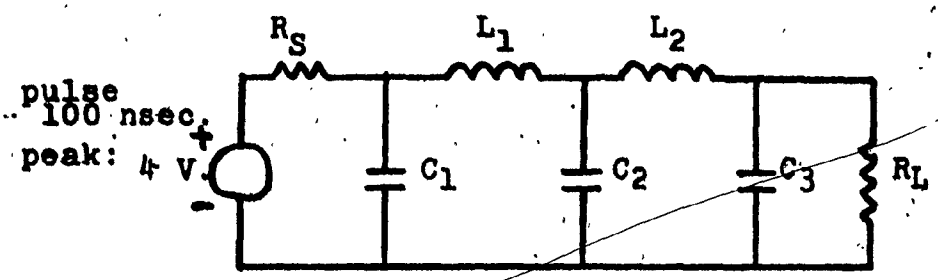
4.4.1 Pulse response of a 5th order low-pass filter

The circuit and element data are shown in Fig. 4.8.

The progedures for program execution is given below:

. Input and circuit analysis sub-program

Step		User action	Display X	Y	Z
1	Press:	END, CONTINUE.	1	1	0
2	Enter:	N = 5, into X-register.	5		
3	Press:	CONTINUE.	1	1	1
4	Enter:	Circuit connection code for shunt (2), capacitor (2) into X- and Y- registers respectively	2	2	
5	Press:	CONTINUE.	1	22	1
6	Enter:	First circuit element value, R = 0, into X-register.	0		
7	Press:	CONTINUE.	2	22	1
8	Enter:	Second circuit element value, L = 0, into X-register.	0		
9	Press:	CONTINUE.	3	22	1
10	Enter:	Third circuit element value, C = 390×10^{-12} farad, into X-register.	390×10^{-12}		
11	Press:	CONTINUE.	2	2	2
	.	The rest of the circuit data are			
	.	entered similarly.			
	.				
12	Press:	CONTINUE.	2	2	0
13	Enter:	R_S = 50, into Y-register,			
		R_L = 50, into X-register.	50	50	
14	Press:	CONTINUE.			
15	Press:	1, PNT, GO TO.			
16	Press:	CONTINUE.			



Circuit element	Description
R_S	91 Ohms
R_L	91 Ohms
C_1	390×10^{-12} farad
C_2	580×10^{-12} farad
C_3	390×10^{-12} farad
L_1	2.2×10^{-9} henry
L_2	2.2×10^{-9} henry

Figure 4.8

Circuit diagram of a 5^{th} order lowpass filter to be excited by a 100 nsec. pulse.

The input data and circuit analysis sub-programs are then being executed. The calculator will stop compution when the total programming steps are executed.

Next to be performed is the system function formation sub-program. In the present example, plotter output and output voltage for a 100 nsec. pulse excitation are chosen.

The program execution procedures are as follows:

. System function formation sub-program

step	User action	Display X	Y	Z
1	Press: 5, FMT, GO TO.	9		
2	Press: END, CONTINUE.	3	3	0
3	Enter: Required system function code, P = 3, into X-register.	3		
4	Press: CONTINUE.	4	4	0
5	Enter: Code for plot routine, 2, into X-register.	2		
6	Press: CONTINUE.	4	4	1
7	Enter: X_0 = 0, into Y-register, X_{scale} = 50×10^{-9} sec/inch, into X-register.	50×10^{-9}	0	
8	Press: CONTINUE.	4	4	1
9	Enter: Y_0 = 0, into Y-register, Y_{scale} = 0.5 volts/inch, into X-register.	0.5	0	
10	Press: CONTINUE.			

The system function formation sub-program is initiated after the complete entry of input data. This sub-program will automatically stop when the computation is completed.

The output response time function computation sub-programs are next loaded according to the procedures in section 4.2. The sub-programs will be initiated by the following commands entered via the calculator keyboard:

CLEAR, 2, FNT, GO TO.
END, CONTINUE.

The input excitation has been pre-programmed to give a 100 nsec. pulse (P10). The output time function is presented in Fig. 4.9. This computed result has been verified experimentally.

4.4.2 The step function response of a second order system

The step response of a simple second order system is chosen for study in the solution accuracy of the program for various sampling intervals.

The circuit, a simple series R-L-C circuit, is excited by a unit step of voltage and the current is defined

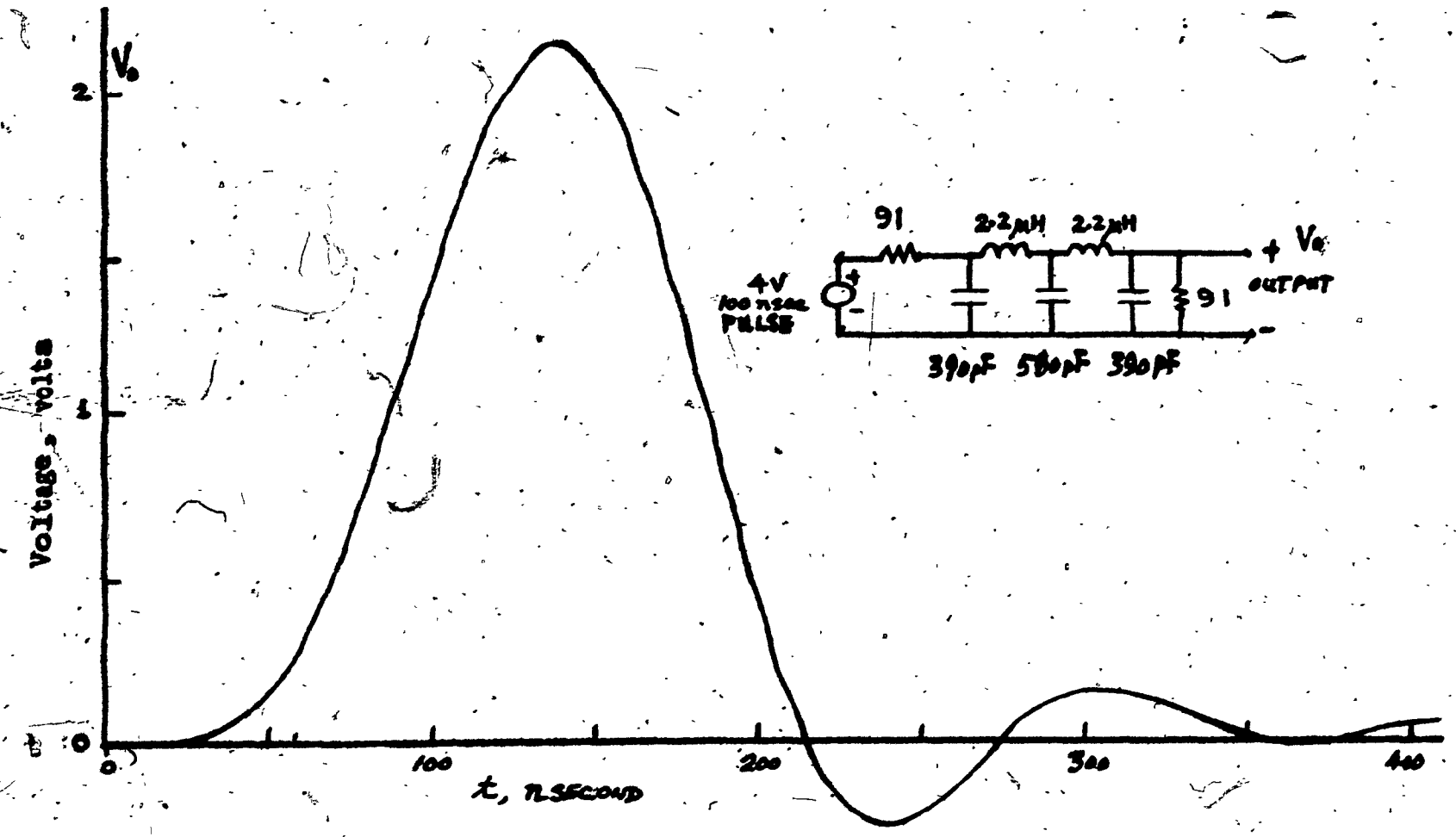
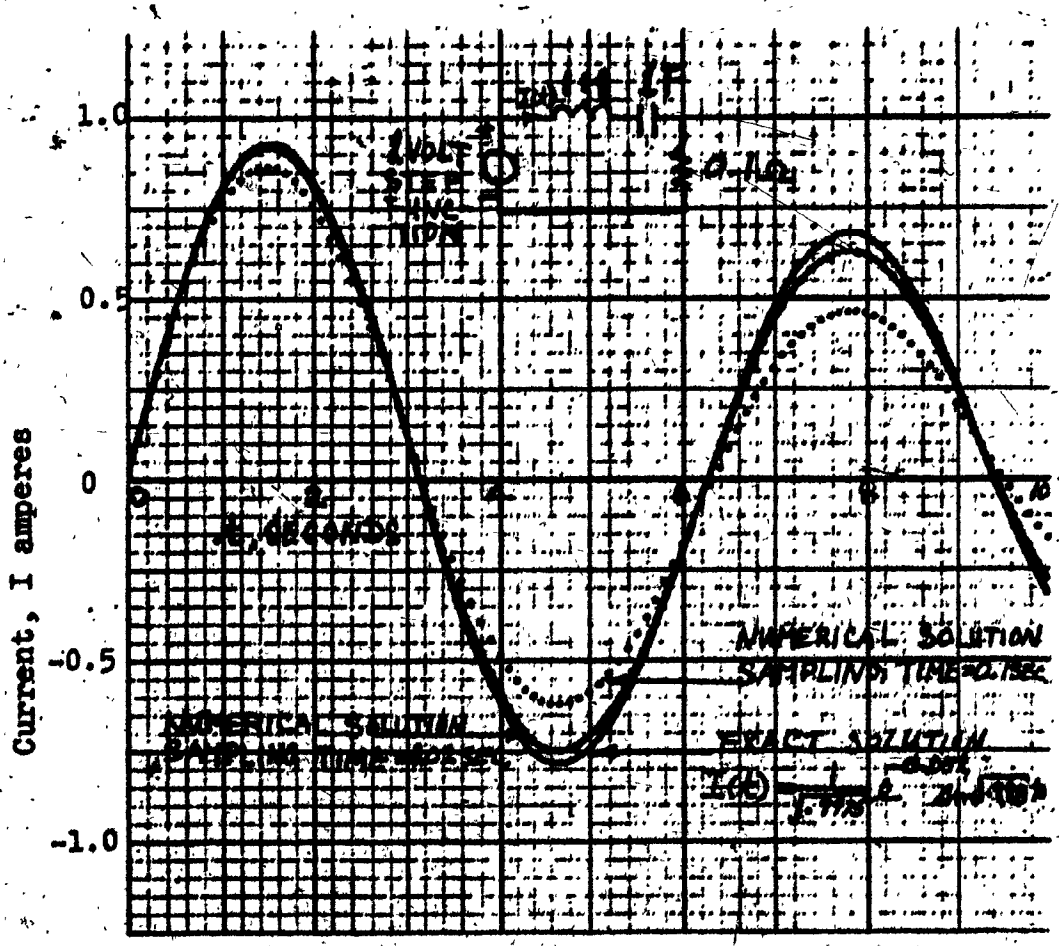


Figure 4.9

Pulse response of a 5th order lowpass filter.

as the response.

Following the procedures of section 4.3, this circuit is loaded into the program. The response time function is plotted for various values of sampling intervals. It is very interesting to note that the numerical solution as shown in Fig. 4.10 readily converges to the exact solution as the sampling interval is decreased from 0.1 second to 0.02 second.



Circuit shown on the graph

Figure 4.10

Step response of a series R-L-C circuit

CHAPTER 5
CONCLUSION

In the preceeding chapters, we have developed and demonstrated that a considerable amount of circuit analysis can be done by a desk-top programmable calculator. The usefulness of these programs are highlighted by the ease of use and the cheap cost of operation.

For the frequency domain circuit analysis program, its analytic power within the cascaded circuit topology has been designed to approach that of a digital computer, except of course for the size of the circuitry to be handled. The practical application value of this program is demonstrated in its being used as a prediction tool in the design of the microwave filter and the wideband amplifier. With good circuit modelling, this program may be used to provide performance calculation to compare with that of experimental breadboard for the purpose of circuit alignment. The effect of a change of circuit component can also be conveniently studied.

As for the improvement of this program, there are two areas which may enhance the analytic power of this program:

. Single element optimization.

While it is understandable that with the existing memory size, it is not possible to perform multi-variable circuit optimization, it seems feasible to at least build in a single variable optimization sub-program. In its simplest form, the performance of the error function will be compared to the variation of a selected circuit component element value until the best compromise is reached. At this time, the particular circuit element value will be finalized and circuit analysis performed accordingly.

. Operator concept of circuit analysis.

One advantage of circuit analysis using matrix approach is the possibility of reducing the task of circuit analysis to matrix manupiiation. In its present form, the program is not able to analyse cascaded circuits with a slight topological change such as the incorporation of series or shunt feedbacks. Consider, for example, the case of shunt feedback by a two-port network, N_2, having the same common ground as the main cascaded circuit which in turn is a cascade of three networks, N_a, N_b, N_c. The

analysis programs in miniature.

In the field of analogue circuit design, the major use of time domain circuit analysis is mostly in the transient analysis of the pulse or step response of filters. Practical applications include the time domain prediction of the filter group-delay, or the examination of the possible spike generation in the biasing circuits of certain sensitive transistors (such as some microwave field-effect transistors). In these applications, the ability to analyse a 9^{th} order system is felt adequate.

The power of the time domain circuit analysis program is fully demonstrated in the examples presented in section 4.4 in which the pulse response of a 5^{th} order low-pass filter is analysed. In general, it is extremely difficult, if not impossible, to analytically evaluate the response function of a high order system even with a simple excitation such as a step or pulse function, not to mention the more complex excitation waveforms. The present program has achieved the capability of accepting random excitation because of the numerical method of solution. While it may be routine practice in digital computers to analyse circuits in the time domain, it is felt that this programming feature is unique in a desk-top calculator program.

The major area requiring improvement is in the speed and accuracy of the calculation. For the moment, the program computation accumulative error is a relative sensitive function of the sampling interval, as can be seen in the second example in section 4.4. Small sampling interval, though gives improvement in solution accuracy, would significantly increase the time required to complete the solution. This problem may be overcome by numerically solving r(KT) implicit in equation 2.4.6 instead of directly solving it from equation 2.4.7.

It is felt, overallwise, that this thesis has served the purpose of pioneering into the possibility of extending the capability of a small memory-sized computer/programmable calculator as a circuit analysis computing tool.

APPENDIX I

FREQUENCY DOMAIN CIRCUIT ANALYSIS PROGRAM

PROGRAMMING STEPS

Title PQ-Frequency Domain Circuit Analysis Input Program

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Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	1	01			
02	↑	27			
03	1	01			
04	→	11			
05	2	02			
06	Acc+	60			
07	1	01			
08	STOP	41			
09	↑	27			
0a	2	02			
0b	0	00			
0c	9	11			
0d	FMT	42			
10	y→	40			
11	y→	40			
12	−	34			
13	d	17			
14	1	01			
15	x→	23			
16	−	34			
17	c	16			
18	2	12			
19	↑	27			
1a	↑	27			
1b	STOP	41			
1c	↑	27			
1d	1	01			
20	0	00			
21	X	36			
22	1	01			
23	+	33			
24	↑	27			
25	FMT	42			
26	y→	40			
27	−	34			
28	1	01			
29	↑	27			
2a	2	02			
2b	0	00			
2c	9	11			
2d	FMT	42			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	STOP	41			
31	↑	27			
32	↑	27			
33	↑	27			
34	x←	67			
35	−	34			
36	c	16			
37	−	34			
38	Roll↓	31			
39	FMT	42			
3a	y→	40			
3b	Roll↑	22			
3c	↑	27			
3d	5	05			
40	x≷y	50			
41	4	04			
42	6	06			
43	1	01			
44	+	33			
45	y→	40			
46	−	34			
47	c	16			
48	GTO	44			
49	2	02			
4a	7	07			
4b	Rcl	61			
4c	x←	67			
4d	−	34			
50	4	04			
51	x≷y	50			
52	÷	24			
53	c	16			
54	1	01			
55	↑	27			
56	FMT	42			
57	y→	40			
58	−	34			
59	1	01			
5a	↑	27			
5b	2	02			
5c	0	00			
5d	9	11			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60	↑	27			
61	1	01			
62	9	11			
63	3	03			
64	Acc+	60			
65	b	00			
66	↑	27			
67	2	02			
68	↑	27			
69	STOP	41			
6a	x→	23			
6b	−	34			
6c	d	17			
6d	2	12			
70	↑	27			
71	↑	27			
72	STOP	41			
73	x→	23			
74	−	34			
75	c	16			
76	↑	27			
77	1	01			
78	0	00			
79	X	36			
7a	↓	25			
7b	+	33			
7c	←	15			
7d	FMT	42			

Memory

Title PO-Continue

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
8 0	y→	40			
1	x←	67			
2	−	34			
3	c	16			
4	f	27			
5	3	03			
6	x≷y	53			
7	b	14			
8	6	06			
9	x≷y	50			
a	a	13			
b	2	02			
c	1	01			
d	f	27			
9 0	2	02			
1	f	27			
2	2	02			
3	STOP	41			
4	f	27			
5	2	02			
6	0	00			
7	0	00			
8	FMT	42			
9	y→	40			
a	1	25			
b	1	01			
c	9	11			
d	9	11			
a 0	FMT	42			
1	y→	40			
2	2	02			
3	f	27			
4	2	02			
5	f	27			
6	2	02			
7	0	00			
8	0	00			
9	FMT	42			
a	y→	40			
b	1	25			
c	1	01			
d	9	11			
b 0	1	25			
1	2	02			
2	0	00			
3	1	01			
4	FMT	42			
5	y→	40			
6	RCL	61			
7	x←	67			
8	−	34			
9	d	17			
a	x≷y	50			
b	c	16			
c	5	05			
d	f	01			
c 0	f	27			
1	asct	60			
2	GoTo	44			
3	6	06			
4	d	17			
5	f	15			
6	f	27			
7	1	01			
8	+	33			
9	9	11			
a	x≷y	30			
b	FMT	42			
c	y→	40			
d	0	00			
d 0	f	27			
1	3	03			
2	f	27			
3	STOP	41			
4	f	27			
5	2	02			
6	0	00			
7	0	00			
8	FMT	42			
9	y→	40			
a	1	25			
b	1	01			
c	9	11			
d	9	11			
e 0	FMT	42			
1	y→	40			
2	2	02			
3	f	27			
4	2	02			
5	f	27			
6	2	02			
7	0	00			
8	0	00			
9	FMT	42			
a	y→	40			
b	1	25			
c	1	01			
d	9	11			
f 0	1	25			
1	2	02			
2	0	00			
3	5	05			
4	FMT	42			
5	y→	40			
6	0	00			
7	f	27			
8	4	04			
9	f	27			
a	STOP	41			
b	x→	23			
c	−	34			
d	c	16			
10 0	2	02			
1	f	27			
2	5	05			
3	FMT	42			
4	y→	40			
5	2	02			
6	4	04			
7	7	07			
8	FMT	42			
9	y→	40			
a	1	25			
b	2	02			
c	f	04			
d	6	06			

Storage

Title PO-Continue.

Step	Key	Code	Display x	Display y	Display z
20	FMT	42			
21	4→	40			
22	X←	67			
23	-	34			
24	C	11			
25	↑	27			
26	2	02			
27	4	04			
28	4	04			
29	FMT	42			
2a	4→	40			
2b	6	06			
2c	↑	27			
2d	↑	27			
30	1	01			
31	STOP	41			
32	FMT	42			
33	G.To	44			
34	END	46			
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
7a					
7b					
7c					
7d					
80					
81					
82					
83					
84					
85					
86					
87					
88					
89					
8a					
8b					
8c					
8d					
90					
91					
92					
93					
94					
95					
96					
97					
98					
99					
9a					
9b					
9c					
9d					
a0					
a1					
a2					
a3					
a4					
a5					
a6					
a7					
a8					
a9					
aa					
ab					
ac					
ad					
b0					
b1					
b2					
b3					
b4					
b5					
b6					
b7					
b8					
b9					
ba					
bb					
bc					
bd					
c0					
c1					
c2					
c3					
c4					
c5					
c6					
c7					
c8					
c9					
ca					
cb					
cc					
cd					
d0					
d1					
d2					
d3					
d4					
d5					
d6					
d7					
d8					
d9					
da					
db					
dc					
dd					
e0					
e1					
e2					
e3					
e4					
e5					
e6					
e7					
e8					
e9					
ea					
eb					
ec					
ed					
f0					
f1					
f2					
f3					
f4					
f5					
f6					
f7					
f8					
f9					
fa					
fb					
fc					
fd					

Title P1-Frequency Domain Circuit Analysis Initialization Program

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	½	01			
03	1	01			
04	FMT	42			
05	X	36			
06	↑	27			
07	2	02			
08	2	02			
09	1	01			
0a	x≷y	50			
0b	1	01			
0c	5	05			
0d	1	01			
10	+	33			
11	½	25			
12	GoTo	44			
13	0	00			
14	4	04			
15	1	01			
16	↑	27			
17	2	02			
18	1	01			
19	0	00			
1a	FMT	42			
1b	R↓	40			
1c	2	02			
1d	2	02			
20	0	00			
21	FMT	42			
22	R↓	40			
23	1	01			
24	3	03			
25	2	02			
26	↑	27			
27	1	01			
28	0	00			
29	8	10			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	8	10			
31	FMT	42			
32	π	56			
33	FMT	42			
34	GoTo	44			
35	2	02			
36	FMT	42			
37	GoTo	44			
38	5	05			
39	FMT	42			
3a	GoTo	44			
3b	2	02			
40	0	00			
41	9	11			
42	FMT	42			
43	π	56			
44	↑	27			
45	1	01			
46	9	11			
47	2	02			
48	↑	27			
49	2	02			
4a	0	00			
4b	8	10			
4c	FMT	42			
4d	π	56			
50	−	34			
51	4	04			
52	+	33			
53	½	25			
54	[illegible]	57			
55	[illegible]	57			
56	[illegible]	50			
57	[illegible]	05			
58	[illegible]	01			
59	[illegible]	00			
5a	[illegible]	10			
5b	[illegible]	42			
5c	[illegible]	44			
5d	[illegible]	02			
60	[illegible]	42			
61	[illegible]	44			
62	[illegible]	02			
63	[illegible]	42			
64	[illegible]	44			
65	[illegible]	02			
66	[illegible]	42			
67	[illegible]	44			
68	[illegible]	02			
69	[illegible]	42			
6a	[illegible]	44			
6b	[illegible]	02			
6c	[illegible]	42			
6d	[illegible]	44			
70	[illegible]	02			
71	[illegible]	42			
72	[illegible]	44			
73	[illegible]	02			
74	[illegible]	42			
75	[illegible]	44			
76	[illegible]	02			
77	[illegible]	42			
78	[illegible]	44			
79	[illegible]	02			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60	3	03			
61	↑	27			
62	2	02			
63	0	00			
64	7	07			
65	FMT	42			
66	R↓	40			
67	2	02			
68	0	00			
69	7	07			
6a	FMT	42			
6b	π	56			
6c	FMT	42			
6d	π	56			
70	↑	27			
71	9	11			
72	x≷y	50			
73	b	14			
74	4	04			
75	1	01			
76	0	00			
77	÷	35			
78	½	25			
79	INT x	64			
7a	x→	25			
7b	−	34			
7c	4	15			
7d	↑	27			

Storage

2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	

Title P1-Continue.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
8 0	1	01			
1	0	00			
2	X	36			
3	2	02			
4	.	00			
5	7	07			
6	FMT	42			
7	π	56			
8	FMT	42			
9	π	56			
a	x⇄y	67			
b	−	34			
c	4	04			
d	0	00			
9 0	+	33			
1	1	25			
2	FMT	42			
3	GoTo	44			
4	x←	67			
5	−	34			
6	1	25			
7	+	33			
8	CONT	47			
9	CONT	47			
a	CONT	47			
b	CONT	47			
c	0	00			
d	x⇄y	50			
A 0	0	00			
1	R↓	10			
2	5	05			
3	0	00			
4	+	33			
5	1	01			
6	FMT	42			
7	GoTo	44			
8	0	00			
9	0	00			
a	1	01			
b	1	01			
c	1	01			
d	1	01			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
b 0	+	33			
1	GoTo	44			
2	6	06			
3	7	07			
4	2	02			
5	4	04			
6	7	07			
7	FMT	42			
8	π	56			
9	↑	27			
a	2	02			
b	4	04			
c	6	06			
d	FMT	42			
C 0	π	56			
1	x⇄y	50			
2	d	17			
3	7	07			
4	x⇄y	50			
5	d	17			
6	7	07			
7	2	02			
8	4	04			
9	4	04			
a	FMT	42			
b	π	56			
c	+	33			
d	2	02			
D 0	4	04			
1	7	07			
2	FMT	42			
3	y→	40			
4	GoTo	44			
5	0	00			
6	0	00			
7	FMT	42			
8	1	01			
9	1	01			
a	1	01			
b	1	01			
c	1	01			
d	1	01			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0	2	02			
1	4	04			
2	5	05			
3	FMT	42			
4	π	56			
5	↑	27			
6	2	02			
7	4	04			
8	7	07			
9	FMT	42			
a	y→	40			
b	END	46			
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Title P2-Complex Number Matrix Multiplication.

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	7	07			
02	↑	27			
03	2	02			
04	1	01			
05	0	00			
06	Occ+	60			
07	2	02			
08	4	04			
09	x→	23			
0a	d	17			
0b	4	04			
0c	FMT	42			
0d	GoTo	44			
10	3	03			
11	FMT	42			
12	GoTo	44			
13	•2	02			
14	4	04			
15	3	03			
16	FMT	42			
17	π	56			
18	↑	27			
19	2	02			
1a	2	02			
1b	7	07			
1c	FMT	42			
1d	y→	40			
20	2	02			
21	4	04			
22	2	02			
23	FMT	42			
24	π	56			
25	↑	27			
26	2	02			
27	2	02			
28	6	06			
29	FMT	42			
2a	y→	40			
2b	Clear	20			
2c	3	03			
2d	↑	27			
30	2	02			
31	2	02			
32	2	02			
33	Occ+	60			
34	1	01			
35	6	06			
36	x→	23			
37	d	17			
38	4	04			
39	FMT	42			
3a	GoTo	44			
3b	3	03			
3c	FMT	42			
3d	GoTo	44			
40	2	02			
41	4	04			
42	3	03			
43	FMT	42			
44	π	56			
45	↑	27			
46	2	02			
47	2	02			
48	9	11			
49	FMT	42			
4a	y→	40			
4b	2	02			
4c	4	04			
4d	2	02			
50	FMT	42			
51	π	56			
52	↑	27			
53	2	02			
54	2	02			
55	3	03			
56	FMT	42			
57	x→	40			
58	Clear	20			
59	3	03			
5a	↑	27			
5b	2	02			
5c	4	04			
5d	2	02			
60	Occ+	60			
61	1	01			
62	6	06			
63	x→	23			
64	d	17			
65	4	04			
66	FMT	42			
67	GoTo	44			
68	3	03			
69	FMT	42			
6a	GoTo	44			
6b	2	02			
6c	4	04			
6d	3	03			
70	FMT	42			
71	π	56			
72	↑	27			
73	2	02			
74	3	03			
75	3	03			
76	FMT	42			
77	y→	40			
78	2	02			
79	4	04			
7a	2	02			
7b	FMT	42			
7c	π	56			
7d	↑	27			

HEWLETT-PACKARD

Title P2-Continue.

Step	Key	Code	Display x	Display y	Display z
8 0	2	02			
1	3	03			
2	2	02			
3	FMT	42			
4	y→	40			
5	Clear	20			
6	3	03			
7	↑	27			
8	2	02			
9	1	01			
a	4	04			
b	Acc+	60			
c	2	02			
d	4	04			
9 0	x→	23			
1	d	17			
2	4	04			
3	FMT	42			
4	GoTo	44			
5	3	03			
6	FMT	42			
7	GoTo	44			
8	2	02			
9	4	04			
a	3	03			
b	FMT	42			
c	π	56			
d	↑	27			
A 0	2	02			
1	3	03			
2	1	01			
3	FMT	42			
4	y→	40			
5	2	02			
6	4	04			
7	2	02			
8	FMT	42			
9	π	56			
a	↑	27			
b	2	02			
c	3	03			
d	0	00			

Step	Key	Code	Display x	Display y	Display z
b 0	FMT	42			
1	y→	40			
2	FMT	42			
3	END	46			
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

5 6 7 8 9 A B C D E

HEWLETT-PACKARD

Title P3-Complex Numbers Multiplication.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	3	03			
03	5	05			
04	FMT	42			
05	π	56			
06	↑	27			
07	2	02			
08	3	03			
09	4	04			
0a	FMT	42			
0b	π	56			
0c	ToPolar	62			
0d	ACCT	60			
10	2	02			
11	3	03			
12	9	11			
13	FMT	42			
14	π	56			
15	↑	27			
16	2	02			
17	3	03			
18	8	10			
19	FMT	42			
1a	π	56			
1b	ToPolar	62			
1c	x↔	23			
1d	d	17			
20	0	00			
21	ACCT	60			
22	RCL	61			
23	↑	27			
24	d	17			
25	X	36			
26	↓	25			
27	ToRect	63			
28	x↔	23			
29	a	13			
2a	4↑	40			
2b	b	14			
2c	Rtn	24			
2d	x	35			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	3	03			
31	7	07			
32	FMT	42			
33	π	56			
34	1	27			
35	2	02			
36	3	03			
37	6	06			
38	FMT	42			
39	π	56			
3a	ToPolar	62			
3b	ACCT	60			
3c	2	02			
3d	4	04			
40	1	01			
41	FMT	42			
42	π	56			
43	↑	27			
44	2	02			
45	4	04			
46	0	00			
47	FMT	42			
48	π	56			
49	ToPolar	62			
4a	x↔	23			
4b	d	17			
4c	a	00			
4d	ACCT	60			
50	RCL	61			
51	↑	27			
52	d	17			
53	X	36			
54	↓	25			
55	ToRect	63			
56	↑	27			
57	a	13			
58	+	33			
59	2	02			
5a	↑	27			
5b	1	01			
5c	FIX	42			
5d	4	04			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60	↓	25			
61	b	14			
62	+	33			
63	2	02			
64	4	04			
65	3	03			
66	FMT	42			
67	4↑	40			
68	FMT	42			
69	RTN	46			
6a					
6b					
6c					
6d					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
7a					
7b					
7c					
7d					

Storage

0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
a	
b	
c	
d	

Title P4-Data Transfer Sub-routine.

Step	Key	Code	Display x	Display y	Display z
00	RCL	61			
01	+	33			
02	y→	40			
03	e	12			
04	f	15			
05	FIX	42			
06	π	56			
07	↑	27			
08	f	15			
09	↑	27			
0a	d	17			
0b	+	33			
0c	1	25			
0d	FIX	42			
10	y→	40			
11	RCL	61			
12	x≷y	50			
13	1	01			
14	c	16			
15	0	00			
16	↑	27			
17	1	01			
18	asct	60			
19	GTO	44			
1a	0	00			
1b	4	04			
1c	FIX	42			
1d	END	42			

Step	Key	Code	Display x	Display y	Display z
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Step	Key	Code	Display x	Display y	Display z
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

Storage

HEWLETT-PACKARD

Title P5-Matrix Data Transfer.

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	3	03			
02	f	27			
03	2	02			
04	.	28			
05	6	06			
06	STO+	60			
07	CyrSkp	32			
08	1	01			
09	6	06			
0a	X→	23			
0b	d	17			
0c	4	04			
0d	FMT	42			
10	GoTo	44			
11	Clear	20			
12	3	03			
13	f	27			
14	2	02			
15	3	03			
16	0	00			
17	STO+	60			
18	CyrSkp	32			
19	1	01			
1a	2	02			
1b	X→	23			
1c	d	17			
1d	4	04			
20	FMT	42			
21	GoTo	44			
22	FMT	42			
23	END	46			

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Storage

0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
a	
b	
c	
d	
e	
f	

HEWLETT-PACKARD

Title P6-Input Data Alteration Program.

Step	Key	Code	Display x	Display y	Display z
0 0	clear	20			
1	6	06			
2	↑	27			
3	↑	27			
4	STOP	41			
5	↑	27			
6	1	01			
7	acct	60			
8	6	15			
9	↑	27			
a	↑	27			
b	STOP	41			
c	↑	27			
d	FIX	42			
1 0	π	56			
1	↑	27			
2	STOP	41			
3	x⇄y	30			
4	↓	25			
5	x⇄y	30			
6	FIX	42			
7	R↓	40			
8	RCL	61			
9	x⇄y	50			
a	2	02			
b	+	04			
c	0	00			
d	↑	27			
2 0	1	01			
1	GTO	44			
2	0	00			
3	7	07			
4	1	01			
5	FIX	42			
6	GTO	44			
7	END	43			

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

F	
E	
D	
C	
B	
A	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

HEWLETT-PACKARD

Title P7-Transistor Scattering Parameters Characterization Input Progra

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	0	00			
03	9	11			
04	FMT	42			
05	π	56			
06	↑	27			
07	4	04			
08	X	36			
09	1	01			
0a	9	11			
0b	2	02			
0c	X≷Y	30			
0d	−	34			
10	Y→	40			
11	d	17			
12	1	01			
13	↑	27			
14	X→	23			
15	C	16			
16	ACCT	60			
17	C	16			
18	RCLL	31			
19	RCL	61			
1a	STOP	41			
1b	↑	27			
1c	d	17			
1d	FMT	42			
20	Y→	40			
21	X≷Y	30			
22	1	01			
23	−	34			
24	1	01			
25	FMT	42			
26	Y→	40			
27	↑	27			
28	1	01			
29	−	34			
2a	Y→	40			
2b	d	17			
2c	1	01			
2d	↑	27			
30	f	15			
31	x≷y	50			
32	3	03			
33	a	13			
34	0	00			
35	↑	27			
36	1	01			
37	GoTo	44			
38	1	01			
39	6	06			
3a	e	12			
3b	x≷y	50			
3c	↑	04			
3d	6	06			
40	1	01			
41	↑	27			
42	GoSqrt	32			
43	GoTo	44			
44	1	01			
45	6	06			
46	C	16			
47	X≷Y	50			
48	5	05			
49	4	04			
4a	Y→	40			
4b	C	16			
4c	Clear	20			
4d	1	01			
50	↑	27			
51	GoTo	44			
52	1	01			
53	6	06			
54	6	06			
55	↑	27			
56	1	01			
57	STOP	41			
58	FMT	42			
59	GoTo	44			
5a	0	00			
5b	0	00			
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					

Storage

F	
E	
D	
C	
B	
A	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

HEWLETT-PACKARD

Title P8-Null Matrix Formation

Step	Key	Code	Display x	Display y	Display z
0 0	Clear	20			
1	2	02			
2	2	02			
3	2	02			
4	↑	27			
5	2	02			
6	1	01			
7	4	04			
8	OCT	60			
9	-0	00			
a	↑	27			
b	ξ	15			
c	FMT	42			
d	X	36			
1 0	e	12			
1	FMT	42			
2	X	36			
3	↑	27			
4	2	02			
5	2	02			
6	5	05			
7	$\sqrt{y}$	50			
8	2	02			
9	1	01			
a	1	01			
b	↑	27			
c	G.To	14			
d	0	00			
2 0	8	10			
1	FMT	42			
2	END	46			
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
1 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
2 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
1 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
2 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Memory

HEWLETT-PACKARD

Title P9-Unity Matrix Formation.

Step	Key	Code	Display x	Display y	Display z
00	8	10			
01	FMT	42			
02	GoTo	44			
03	1	01			
04	↑	27			
05	2	02			
06	1	01			
07	4	04			
08	FMT	42			
09	y→	40			
0a	2	02			
0b	2	02			
0c	4	04			
0d	FMT	42			
10	y→	40			
11	FMT	42			
12	END	46			
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
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15					
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1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
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1a					
1b					
1c					
1d					
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24					
25					
26					
27					
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2a					
2b					
2c					
2d					

HEWLETT-PACKARD

HEWLETT-PACKARD

HEWLETT-PACKARD

HEWLETT-PACKARD

Title Pi-Series Resistance, R_s.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	9	11			
01	FIXT	42			
02	GoTo	44			
03	4	04			
04	↑	27			
05	2	02			
06	0	03			
07	8	10			
08	FIXT	42			
09	−	34			
0a	FIXT	42			
0b	π	56			
0c	↑	27			
0d	3	03			
10	+	33			
11	↓	25			
12	FIXT	42			
13	π	56			
14	↑	27			
15	2	02			
16	2	02			
17	2	02			
18	FIXT	42			
19	÷	40			
1a	FIXT	42			
1b	END	46			
1c					
1d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					

Memory

0	
1	
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a	
b	
c	
d	
e	
f	

Title R12-Series Connected Series R-L-C

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	9	11			
01	FIX	42			
02	GTO	44			
03	CHS	20			
04	4	04			
05	↑	27			
06	2	02			
07	0	00			
08	8	10			
09	FIX	42			
0a	−	34			
0b	FIX	42			
0c	π	56			
0d	x↔y	23			
10	d	17			
11	↑	27			
12	3	03			
13	+	33			
14	1	25			
15	FIX	42			
16	π	56			
17	↑	27			
18	2	02			
19	2	02			
1a	2	02			
1b	FIX	42			
1c	y^x	40			
1d	2	02			
20	+	33			
21	7	07			
22	FIX	42			
23	π	56			
24	↑	27			
25	2	02			
26	2	02			
27	2	02			
28	FIX	42			
29	y^x	40			
2a	2	02			
2b	+	33			
2c	RCL	61			
2d	0	00			
30	+	33			
31	↓	25			
32	FIX	42			
33	π	56			
34	X	36			
35	0	00			
36	OCT	60			
37	1	01			
38	↑	27			
39	↑	27			
3a	d	17			
3b	+	33			
3c	↓	25			
3d	FIX	42			
40	π	56			
41	↓	25			
42	↓	25			
43	÷	35			
44	0	00			
45	GTO	63			
46	RCL	61			
47	2	02			
48	2	02			
49	3	03			
4a	FIX	42			
4b	y^x	40			
4c	FIX	42			
4d	END	62			
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					

Storage

Title P13-Series Connected Parallel R-L-C.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	3	03			
02	FMT	42			
03	GoTo	44			
04	9	09			
05	0	00			
06	FMT	42			
07	GoTo	44			
08	FMT	42			
09	END	46			
0a					
0b					
0c					
0d					
0e					
0f					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
1e					
1f					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					
2e					
2f					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					
3e					
3f					
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					
4e					
4f					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					
5e					
5f					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					
6e					
6f					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
7a					
7b					
7c					
7d					
7e					
7f					
80					
81					
82					
83					
84					
85					
86					
87					
88					
89					
8a					
8b					
8c					
8d					
8e					
8f					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
90					
91					
92					
93					
94					
95					
96					
97					
98					
99					
9a					
9b					
9c					
9d					
9e					
9f					
a0					
a1					
a2					
a3					
a4					
a5					
a6					
a7					
a8					
a9					
aa					
ab					
ac					
ad					
ae					
af					
b0					
b1					
b2					
b3					
b4					
b5					
b6					
b7					
b8					
b9					
ba					
bb					
bc					
bd					
be					
bf					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
c0					
c1					
c2					
c3					
c4					
c5					
c6					
c7					
c8					
c9					
ca					
cb					
cc					
cd					
ce					
cf					
d0					
d1					
d2					
d3					
d4					
d5					
d6					
d7					
d8					
d9					
da					
db					
dc					
dd					
de					
df					
e0					
e1					
e2					
e3					
e4					
e5					
e6					
e7					
e8					
e9					
ea					
eb					
ec					
ed					
ee					
ef					

Title #14-Series Connected Open-Circuited Transmission Line.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	4	04			
02	Fix	42			
03	GoTo	44			
04	9	11			
05	0	00			
06	Fix	42			
07	GoTo	44			
08	Fix	42			
09	End	46			
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P15-Series Connected Short-Circuited Transmission Line.

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	5	05			
02	FIXT	42			
03	GoTo	44			
04	·9	11			
05	0	00			
06	FIXT	42			
07	GoTo	44			
08	FIXT	42			
09	END	46			
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					

Storage

0e	
0d	
0c	
0b	
0a	
09	
08	
07	
06	
05	
04	
03	
02	
01	
00	

Title P21-Parallel Shunt resistance, R_p

Step	Key	Code	Display x	Display y	Display z
00	9	11			
01	FMT	42			
02	GoTo	44			
03	1	01			
04	↑	27			
05	4	04			
06	↑	27			
07	2	02			
08	0	00			
09	8	10			
0a	FMT	42			
0b	−	34			
0c	FMT	42			
0d	π	56			
10	X≷Y	30			
11	3	03			
12	+	33			
13	↓	25			
14	FMT	42			
15	π	56			
16	÷	35			
17	2	02			
18	1	01			
19	6	06			
1a	FMT	42			
1b	Y→	40			
1c	FMT	42			
1d	END	46			

Step	Key	Code	Display x	Display y	Display z
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

Step	Key	Code	Display x	Display y	Display z
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Storage
f
e
d
c
b
9
8
7
6
5
4
3
2
1
0

HEWLETT-PACKARD

Title P22-Shunt Connected Series R-L-C.

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
0	1	01			
1	2	02			
2	FMT	42			
3	GoTo	44			
4	9	11			
5	1	01			
6	FMT	42			
7	GoTo	44			
8	FMT	42			
9	END	46			
a					
b					
c					
d					

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P23-Shunt Connected Parallel R-L-C.

Step	Key	Code	Display x	Display y	Display z
00	9	11			
01	FMT	42			
02	G→To	44			
03	Clear	20			
04	2	02			
05	4	04			
06	7	07			
07	FMT	42			
08	π	56			
09	↑	27			
0a	2	02			
0b	X	36			
0c	π	56			
0d	X	36			
10	y→	40			
11	C	16			
12	4	04			
13	↑	27			
14	2	02			
15	0	00			
16	8	10			
17	FMT	42			
18	−	34			
19	FMT	42			
1a	π	56			
1b	x→	23			
1c	d	17			
1d	↑	27			
20	2	02			
21	+	33			
22	↓	25			
23	FMT	42			
24	π	56			
25	↑	27			
26	C	16			
27	X	36			
28	4	04			
29	↑	27			
2a	2	02			
2b	+	33			
2c	↓	25			
2d	FMT	42			

Step	Key	Code	Display x	Display y	Display z
30	π	56			
31	To Polar	62			
32	X⇄Y	30			
33	Op Sign	32			
34	↑	27			
35	1	01			
36	Roll ↑	22			
37	÷	35			
38	↓	25			
39	To Rect	66			
3a	acc+	60			
3b	d	17			
3c	↑	27			
3d	1	01			
40	(+)	33			
41	↓	25			
42	FMT	42			
43	π	56			
44	↑	27			
45	C	16			
46	X	36			
47	0	00			
48	acc+	60			
49	Rcl	61			
4a	↑	27			
4b	2	02			
4c	1	01			
4d	6	06			
50	FMT	42			
51	y→	40			
52	↓	25			
53	2	02			
54	↓	25			
55	7	07			
56	FMT	42			
57	y→	40			
58	FMT	42			
59					
5a					
5b					
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
7a					
7b					
7c					
7d					

Storage

0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
a	
b	
c	
d	
e	
f	

HEWLETT-PACKARD

Title P24-Shunt Connected Open-Circuited Transmission Line.

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	5	05			
02	FMT	42			
03	GoTo	44			
04	2	02			
05	0	00			
06	R/S	51			
07	FMT	42			
08	π	56			
09	↑	27			
0a	2	02			
0b	+	33			
0c	↓	25			
0d	FMT	42			
10	π	56			
11	x→	23			
12	d	17			
13	clear	20			
14	2	02			
15	1	01			
16	7	07			
17	FMT	42			
18	π	56			
19	↑	27			
1a	2	02			
1b	1	01			
1c	6	06			
1d	FMT	42			
20	π	56			
21	Fib	61			
22	x≷y	30			
23	4→R	31			
24	1	01			
25	1	01			
26	Rdn	32			
27	-	34			
28	1	01			
29	+	33			
2a	1	01			
2b	÷	24			
2c	2	02			
2d	÷	24			

Step	Key	Code	Display x	Display y	Display z
10	2	02			
11	1	01			
12	6	06			
13	FMT	42			
14	y→	40			
15	↓	25			
16	2	02			
17	1	01			
18	7	07			
19	FMT	42			
1a	y→	40			
1b	FMT	42			
1c	END	46			
1d					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					

Step	Key	Code	Display x	Display y	Display z
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					

Storage

Title P25-Shunt Connected Short-Circuited Transmission Line.

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
0 0	9	11			
1	FIX	42			
2	GoTo	44			
3	Clear	20			
4	.4	04			
5	↑	27			
6	2	02			
7	0	00			
8	B	LD			
9	FIX	42			
a	−	34			
b	FIX	42			
c	π	56			
d	X→	23			
1 0	d	17			
1	↑	27			
2	3	03			
3	+	33			
4	↓	25			
5	FIX	42			
6	π	56			
7	↑	27			
8	2	02			
9	↑	04			
a	7	07			
b	FIX	42			
c	π	56			
d	X	36			
2 0	2	02			
1	X	36			
2	π	56			
3	X	36			
4	1	01			
5	1	01			
6	B	LD			
7	Exp	24			
8	1	01			
9	0	00			
a	÷	35			
b	Ln	13			

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
3 0	↑	27			
1	1	01			
2	+	33			
3	↓	25			
4	FIX	42			
5	π	56			
6	↑	27			
7	2	02			
8	X	36			
9	a	13			
a	x⇄y	30			
b	÷	35			
c	R↓	40			
d	G−	16			
4 0	a	13			
1	Tan X	71			
2	x⇄y	30			
3	Hyper	67			
4	Tan X	71			
5	↑	27			
6	↓	25			
7	To Polar	62			
8	Ln X	65			
9	Acc−	63			
a	↓	25			
b	C	16			
c	Hyper	67			
d	Tan X	71			
5 0	X	36			
1	1	01			
2	To Polar	62			
3	Ln X	65			
4	Acc+	40			
5	d	17			
6	↑	27			
7	2	02			
8	+	33			
9	↓	25			
a	FIX	42			
b	π	56			
c	↑	27			

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
6 0	X²	74			
1	X⇄y	30			
2	÷	35			
3	e	12			
4	X⇄y	30			
5	To Rect	66			
6	↑	27			
7	2	02			
8	1	01			
9	6	06			
a	FIX	42			
b	R↓	40			
c	↓	25			
d	2	02			
7 0	1	01			
1	7	07			
2	FIX	42			
3	R↓	40			
4	FIX	42			
5	END	46			
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	

Title P90-Program For: $a_{12}=1/a_{21}$, and set $a_{21}=0$.

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	1	01			
02	7	07			
03	FMT	42			
04	π	56			
05	↑	27			
06	2	02			
07	1	01			
08	6	06			
09	FMT	42			
0a	π	56			
0b	To Polar	62			
0c	x≷1	30			
0d	Op Sign	32			
10	↑	27			
11	1	01			
12	Roll↑	22			
13	÷	35			
14	↓	25			
15	To Rect	66			
16	↑	27			
17	2	02			
18	2	02			
19	2	02			
1a	FMT	42			
1b	y→	40			
1c	↓	25			
1d	2	02			
20	2	02			
21	3	03			
22	FMT	42			
23	y→	40			
24	Clx	20			
25	2	02			
26	1	01			
27	6	06			
28	FMT	42			
29	y→	40			
2a	2	02			
2b	1	01			
2c	7	07			
2d					

Step	Key	Code	Display x	Display y	Display z
30	y→	40			
31	FMT	42			
32	END	46			
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
a	
b	
c	
d	
e	
f	

HEWLETT-PACKARD

Title P91-Program for: $a_{21} = 1/a_{12}$, and set $a_{12} = 0$.

HEWLETT-PACKARD (22)

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	2	02			
02	3	03			
03	FMT	42			
04	π	56			
05	↑	27			
06	2	02			
07	2	02			
08	2	02			
09	FMT	42			
0a	π	56			
0b	ToPolar	62			
0c	x↔y	30			
0d	R↓	32			

HEWLETT-PACKARD (23)

Step	Key	Code	Display x	Display y	Display z
10	↑	27			
11	1	01			
12	RollUp	22			
13	÷	35			
14	↓	25			
15	ToRect	66			
16	↑	27			
17	2	02			
18	1	01			
19	6	06			
1a	FMT	42			
1b	4→	40			
1c	↓	25			
1d	2	02			

HEWLETT-PACKARD (24)

Step	Key	Code	Display x	Display y	Display z
20	1	01			
21	7	07			
22	FMT	42			
23	4→	40			
24	Chs	20			
25	2	02			
26	2	02			
27	2	02			
28	FMT	42			
29	4→	40			
2a	2	02			
2b	2	02			
2c	3	03			
2d	FMT	42			

HEWLETT-PACKARD (25)

Step	Key	Code	Display x	Display y	Display z
30	4→	40			
31	FMT	42			
32	END	46			
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

HEWLETT-PACKARD (26)

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
a	
b	
c	
d	

Title P36-Cascaded Connected Transmission Line.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	4	04			
01	↑	27			
02	2	02			
03	0	00			
04	8	LO			
05	FIX	42			
06	−	34			
07	FIX	42			
08	π	35			
09	x→	23			
0a	d	L7			
0b	↑	27			
0c	3	03			
0d	+	33			
10	↓	25			
11	FIX	42			
12	π	56			
13	↑	27			
14	2	02			
15	4	04			
16	7	07			
17	FIX	42			
18	π	56			
19	X	36			
1a	2	02			
1b	X	36			
1c	π	56			
1d	X	36			
20	1	01			
21	1	01			
22	8	LO			
23	Sto	16			
24	1	01			
25	0	00			
26	÷	35			
27	y→	40			
28	c	16			
29	d	L7			
2a	↑	27			
2b	[illegible]	01			
2c	[illegible]	35			
2d	[illegible]	[illegible]			

Step	Key	Code	Display x	Display y	Display z
30	FIX	42			
31	π	56			
32	x→	23			
33	↑	15			
34	d	L7			
35	↑	27			
36	1	01			
37	+	33			
38	↓	25			
39	FIX	42			
3a	π	56			
3b	x→	23			
3c	e	L2			
3d	c	L6			
40	↑	27			
41	2	02			
42	÷	35			
43	e	L2			
44	÷	35			
45	y→	40			
46	e	L2			
47	↓	15			
48	hyper	67			
49	Cos x	73			
4a	↑	27			
4b	c	L6			
4c	Cos x	73			
4d	X	36			
50	2	02			
51	1	01			
52	↑	04			
53	FIX	42			
54	y→	40			
55	2	02			
56	2	02			
57	4	04			
58	FIX	42			
59	y→	40			
5a	c	L6			
5b	Sin x	70			
5c	↑	27			
5d	[illegible]	[illegible]			

Step	Key	Code	Display x	Display y	Display z
60	hyper	67			
61	Sin x	70			
62	X	36			
63	2	02			
64	1	01			
65	5	05			
66	FIX	42			
67	y→	40			
68	2	02			
69	2	02			
6a	5	05			
6b	FIX	42			
6c	y→	40			
6d	c	L6			
70	Cos x	73			
71	↑	27			
72	e	L2			
73	hyper	67			
74	Sin x	70			
75	X	36			
76	↑	15			
77	X	36			
78	2	02			
79	2	02			
7a	2	02			
7b	FIX	42			
7c	y→	40			
7d	↑	15			

Storage	
f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P36-Continue.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
8 0	(÷	35			
1	÷	35			
2	2	02			
3	1	01			
4	.6	06			
5	FIX	42			
6	y→	40			
7	c	16			
8	SIN X	70			
9	f	27			
a	e	12			
b	hyper	67			
c	Cos X	73			
d	X	36			
9 0	(	15			
1	X	36			
2	2	02			
3	2	02			
4	)	03			
5	FIX	42			
6	y→	40			
7	(	15			
8	÷	35			
9	÷	35			
a	2	02			
b	1	01			
c	7	07			
d	FIX	42			
a 0	y→	40			
1	FIX	42			
2	END	46			
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					o
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

F	
E	
D	
C	
B	
A	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P37-Cascaded Connected Transformer.

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
0	8	10			
1	FMT	42			
2	GoTo	44			
3	4	04			
4	↑	27			
5	2	02			
6	0	00			
7	8	10			
8	FMT	42			
9	−	34			
a	FMT	42			
b	π	56			
c	↑	27			
d	3	03			

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
0	+/−	33			
1	↓	25			
2	FMT	42			
3	π	56			
4	↑	27			
5	1	01			
6	x≷y	30			
7	÷	35			
8	↑	27			
9	2	02			
a	2	02			
b	4	04			
c	FMT	42			
d	R↓	40			

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
0	↓	25			
1	2	02			
2	L	01			
3	4	04			
4	FMT	42			
5	R↓	40			
6	FMT	42			
7	R↓	40			
8					
9					
a					
b					
c					
d					

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Memory

0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
a	
b	
c	
d	
e	

Title P38-Cascade Connected Inverter.

Step	Key	Code	Display x	Display y	Display z
00	B	10			
01	FMT	42			
02	GoTo	44			
03	4	04			
04	↑	27			
05	2	02			
06	0	00			
07	B	10			
08	FMT	42			
09	−	34			
0a	FMT	42			
0b	π	56			
0c	↑	27			
0d	3	03			
10	+	33			
11	↓	25			
12	FMT	42			
13	π	56			
14	↑	27			
15	1	01			
16	x≷y	30			
17	÷	35			
18	↑	27			
19	2	02			
1a	2	02			
1b	2	02			
1c	FMT	42			
1d	R↓	40			
20	↓	25			
21	2	02			
22	1	01			
23	6	06			
24	FMT	42			
25	R↓	40			
26	FIX	43			
27	END	00			

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					

Storage

0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
a	
b	
c	
d	
e	

HEWLETT-PACKARD

Title P39-Transistor Common-Emitter Hybrid π Model(r_{be} not included).

Step	Key	Code	Display x	Display y	Display z
0 0	Clear	20			
1	4	04			
2	↑	27			
3	2	02			
4	0	00			
5	B	10			
6	FMT	42			
7	−	34			
8	FMT	42			
9	π	56			
a	X→	23			
b	d	17			
c	↑	27			
d	1	01			
1 0	+	33			
1	↓	25			
2	FMT	42			
3	π	56			
4	↑	27			
5	2	02			
6	X	36			
7	π	56			
8	X	36			
9	2	02			
a	4	04			
b	7	07			
c	FMT	42			
d	π	56			
2 0	X	36			
1	Y→	40			
2	c	16			
3	1	01			
4	↑	27			
5	d	17			
6	↑	27			
7	2	02			
8	+	33			
9	↓	25			
a	FMT	42			
b	π	56			
c	÷	35			
d	Y→	40			

Step	Key	Code	Display x	Display y	Display z
3 0	b	14			
1	d	17			
2	↑	27			
3	3	03			
4	+	33			
5	↓	25			
6	FMT	42			
7	π	56			
8	X→	23			
9	a	13			
a	−	34			
b	c	16			
c	X⇄Y	30			
d	To Polar	62			
4 0	LnX	65			
1	CLx	63			
2	RCL	61			
3	e^x	74			
4	To Rect	66			
5	↑	27			
6	2	02			
7	2	02			
8	2	02			
9	FMT	42			
a	Y→	40			
b	↓	25			
c	2	02			
d	2	02			
5 0	3	03			
1	FMT	42			
2	Y→	40			
3	c	16			
4	↑	27			
5	↓	25			
6	To Polar	66			
7	LnX	65			
8	CLx	63			
9	RCL	61			
a	e^x	74			
b	↑	27			
c	1	01			
d	X	36			

Step	Key	Code	Display x	Display y	Display z
6 0	1	01			
1	4	04			
2	FMT	42			
3	Y→	40			
4	2	02			
5	2	02			
6	4	04			
7	FMT	42			
8	Y→	40			
9	↓	25			
a	2	02			
b	1	01			
c	5	05			
d	FMT	42			
7 0	Y→	40			
1	2	02			
2	2	02			
3	5	05			
4	FMT	42			
5	Y→	40			
6	RCL	61			
7	e^x	74			
8	↑	27			
9	a	13			
a	X	36			
b	↓	25			
c	To Rect	66			
d	↑	27			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

HEWLETT-PACKARD

Title P39-Continue.

Step	Key	Code	Display x	Display y	Display z
0	2	02			
1	1	01			
2	6	06			
3	FIX	42			
4	y→	40			
5	↓	25			
6	2	02			
7	1	01			
8	7	07			
9	FIX	42			
a	y→	40			
b	FIX	42			
c	END	46			
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage
f
e
d
c
b
a
9
8
7
6
5
4
3
2
1
0

Title P33-Cascaded Circuit Block, Scattering Parameters Characterizatio

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
00	4	04			
01	f	27			
02	2	02			
03	0	00			
04	8	10			
05	Fix	42			
06	−	34			
07	Fix	42			
08	π	56			
09	↑	27			
0a	2	02			
0b	+	33			
0c	1	01			
0d	x⇄y	30			
10	+	33			
11	Fix	42			
12	π	56			
13	x⇄y	30			
14	Fix	42			
15	π	56			
16	x→	23			
17	c	16			
18	y→	40			
19	d	17			
1a	Clear	20			
1b	1	01			
1c	9	11			
1d	2	02			
20	↑	27			
21	2	02			
22	0	00			
23	9	11			
24	Fix	42			
25	π	56			
26	f	27			
27	4	04			
28	X	36			
29	1	01			
2a	−	34			
2b	2	02			
2c	2	02			
2d	6	06			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
30	acc+	60			
31	e	12			
32	↑	27			
33	Fix	42			
34	π	56			
35	x→	23			
36	b	14			
37	8	10			
38	−	34			
39	↓	25			
3a	Fix	42			
3b	π	56			
3c	x→	23			
3d	a	13			
40	9	11			
41	5	05			
42	Fix	42			
43	Gōto	44			
44	a	13			
45	↑	27			
46	f	15			
47	Fix	42			
48	y→	40			
49	f	15			
4a	↑	27			
4b	2	02			
4c	3	03			
4d	3	03			
50	x⇄y	50			
51	5	05			
52	a	13			
53	1	01			
54	↑	27			
55	[illegible]	[illegible]			
56	[illegible]	[illegible]			
57	[illegible]	[illegible]			
58	[illegible]	[illegible]			
59	[illegible]	[illegible]			
5a	[illegible]	[illegible]			
5b	[illegible]	[illegible]			
5c	[illegible]	[illegible]			
5d	[illegible]	[illegible]			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
60	↑	27			
61	1	01			
62	8	10			
63	0	00			
64	acc+	60			
65	e	12			
66	Fix	42			
67	π	56			
68	↑	27			
69	1	01			
6a	÷	35			
6b	π	56			
6c	X	36			
6d	e	12			
70	Fix	42			
71	g→	40			
72	↑	27			
73	2	02			
74	3	03			
75	3	03			
76	x⇄y	50			
77	8	10			
78	1	01			
79	2	02			
7a	↑	27			
7b	0	00			
7c	Gōto	44			
7d	6	06			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P33-Continue.

Step	Key	Code	Display x	Display y	Display z
8 0	4	04			
1	9	11			
2	4	04			
3	FIT	42			
4	GoTo	44			
5	FIT	42			
6	END	46			
7					
8					
9					
a					
b					
c					
d					
9 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f
e
d
c
b
a
9
8
7
6
5
4
3
2
1
0

HEWLETT-PACKARD 67
HEWLETT-PACKARD 97
HEWLETT-PACKARD 97
HEWLETT-PACKARD

Title P92-Sub-routine To Compute $\left(\frac{AB}{a_{32}a_{21}} + \frac{g_{12}}{2}\right)$ For P94.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	X←	67			
02	–	34			
03	6	06			
04	↑	27			
05	X←	67			
06	–	34			
07	7	07			
08	LnX	65			
09	acc+	60			
0a	X←	67			
0b	–	34			
0c	8	10			
0d	↑	27			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
10	X←	67			
11	–	34			
12	9	11			
13	LnX	65			
14	acc+	60			
15	2	02			
16	3	03			
17	1	01			
18	FIX	42			
19	π	56			
1a	↑	27			
1b	2	02			
1c	3	03			
1d	0	00			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
20	FIX	42			
21	π	56			
22	↑	27			
23	2	02			
24	X	36			
25	1	25			
26	LnX	65			
27	acc-	63			
28	Rcl	61			
29	acc-	63			
2a	÷	24			
2b	Rcl	61			
2c	acc+	60			
2d	↑	27			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	2	02			
31	9	11			
32	FIX	42			
33	π	56			
34	↑	27			
35	2	02			
36	2	02			
37	8	10			
38	FIX	42			
39	π	56			
3a	↑	27			
3b	2	02			
3c	÷	35			
3d	↓	25			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
40	To Rect	66			
41	acc+	60			
42	Rcl	61			
43	X→	23			
44	–	34			
45	5	05			
46	Y→	40			
47	–	34			
48	4	04			
49	FIX	42			
4a	END	46			
4b					
4c					
4d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					

Storage	
f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P93-Sub-routine To Compute $\left(\frac{AB}{2S_{24}} - \frac{S_{12}}{2}\right)^{\frac{1}{2}}$ For P94.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0 0	Clear	20			
0 1	x←	67			
0 2	−	34			
0 3	6	06			
0 4	↑	27			
0 5	x←	67			
0 6	−	34			
0 7	7	07			
0 8	lnx	65			
0 9	acc+	60			
0 a	x←	67			
0 b	−	34			
0 c	8	10			
0 d	↑	27			
1 0	x←	67			
1 1	−	34			
1 2	9	11			
1 3	lnx	65			
1 4	acc+	60			
1 5	2	02			
1 6	3	03			
1 7	1	01			
1 8	FMT	42			
1 9	π	56			
1 a	↑	27			
1 b	2	02			
1 c	3	03			
1 d	0	00			
2 0	FMT	42			
2 1	π	56			
2 2	↑	27			
2 3	2	02			
2 4	X	36			
2 5	↓	25			
2 6	lnx	65			
2 7	acc−	63			
2 8	Rcl	61			
2 9	acc−	63			
2 a	x²	34			
2 b	ToRect	66			
2 c	acc+	60			
2 d	2	02			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
3 0	2	02			
3 1	9	11			
3 2	FMT	42			
3 3	π	56			
3 4	↑	27			
3 5	2	02			
3 6	2	02			
3 7	8	10			
3 8	FMT	42			
3 9	π	56			
3 a	↑	27			
3 b	2	02			
3 c	÷	35			
3 d	↓	25			
4 0	ToRect	66			
4 1	acc−	63			
4 2	Rcl	61			
4 3	acc−	63			
4 4	ToPolar	62			
4 5	acc+	60			
4 6	5	05			
4 7	0	00			
4 8	↑	27			
4 9	6	15			
4 a	x^y	30			
4 b	÷	35			
4 c	-2	12			
4 d	x^y	30			
5 0	ToRect	66			
5 1	x↔	23			
5 2	−	34			
5 3	5	05			
5 4	y↑	40			
5 5	−	34			
5 6	4	04			
5 7	FMT	42			
5 8	END	46			
5 9					
5 a					
5 b					
5 c					
5 d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
b	
c	
d	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P94-Conversion of Scattering Parameters To Chain Matrix.

HEWLETT·PACKARD 25 HEWLETT·PACKARD 65 HEWLETT·PACKARD 67/97

Step	Key	Code	Display x	Display y	Display z
0 0	2	02			
1	2	02			
2	7	07			
3	Fπ	42			
4	π	56			
5	↑	27			
6	2	02			
7	2	02			
8	6	06			
9	Fπ	42			
a	π	56			
b	To Rect	66			
c	↑	27			
d	1	01			
1 0	+	33			
1	↓	25			
2	To Polar	62			
3	x→	23			
4	−	34			
5	4	15			
6	y→	40			
7	−	34			
8	=	12			
9	To Rect	66			
a	x⇄y	30			
b	CHS	32			
c	↑	27			
d	2	02			
2 0	Roll↑	22			
1	−	34			
2	↓	25			
3	To Polar	62			
4	x→	23			
5	−	34			
6	4	15			
7	y→	40			
8	−	34			
9	=	12			
a	2	02			
b	CHS	32			
c	↑	27			
d	2	02			
3 0	π	56			
1	↑	27			
2	2	02			
3	3	03			
4	2	02			
5	Fπ	42			
6	π	56			
7	To Rect	66			
8	↑	27			
9	1	01			
a	+	33			
b	↓	25			
c	To Polar	62			
d	x→	23			
4 0	−	34			
1	b	14			
2	y→	40			
3	−	34			
4	a	12			
5	To Rect	66			
6	x⇄y	30			
7	CHS	32			
8	↑	27			
9	2	02			
a	Roll↑	22			
b	−	34			
c	↓	25			
d	To Polar	62			
5 0	x→	23			
1	−	34			
2	9	11			
3	y→	40			
4	−	34			
5	8	10			
6	x←	67			
7	−	34			
8	4	15			
9	x→	23			
a	−	34			
b	7	07			
c	x←	67			
d	2	02			
6 0	C	16			
1	x→	23			
2	−	34			
3	6	06			
4	9	11			
5	3	03			
6	Fπ	42			
7	Goto	44			
8	y⇄z	24			
9	−	34			
a	5	05			
b	2	02			
c	1	01			
d	6	06			
7 0	Fπ	42			
1	y→	40			
2	y⇄z	24			
3	−	34			
4	4	04			
5	2	02			
6	1	01			
7	7	07			
8	Fπ	42			
9	y→	40			
a	x←	67			
b	−	34			
c	4	15			
d	x→	23			

Storage

f															
e															
d															
c															
b															
a															
9															
8															
7															
6															
5															
4															
3															
2															
1															
0															

Title P94-Continue.

Step	Key	Code	Display x	Display y	Display z
8 0	−	34			
1	7	07			
2	x←	67			
3	−	34			
4	2	12			
5	x→	23			
6	−	34			
7	6	06			
8	9	11			
9	2	02			
a	FMT	42			
b	GoTo	44			
c	y≷	24			
d	−	34			
9 0	5	05			
1	2	02			
2	1	01			
3	4	04			
4	FMT	42			
5	y→	40			
6	y≷	24			
7	−	34			
8	4	04			
9	2	02			
a	1	01			
b	5	05			
c	FMT	42			
d	y→	40			
a 0	x←	67			
1	−	34			
2	6	14			
3	x→	23			
4	−	34			
5	9	11			
6	x←	67			
7	−	34			
8	0	13			
9	x→	23			
a	−	34			
b	8	10			
c	9	11			
d	3	03			

Step	Key	Code	Display x	Display y	Display z
b 0	FMT	42			
1	GoTo	44			
2	y≷	24			
3	−	34			
4	4	04			
5	x←	67			
6	−	34			
7	5	05			
8	To Polar	62			
9	↑	27			
a	5	05			
b	0	00			
c	X	36			
d	X	36			
c 0	↓	25			
1	To Rect	66			
2	↑	27			
3	2	02			
4	2	02			
5	2	02			
6	FMT	42			
7	y→	40			
8	↓	25			
9	2	02			
a	2	02			
b	3	03			
c	FMT	42			
d	y→	40			
d 0	x←	67			
1	−	34			
2	d	17			
3	x→	23			
4	−	34			
5	7	07			
6	GoTo	44			
7	−	34			
8	0	00			
9	0	00			
a	Const	47			
b	Const	47			
c	Const	47			
d	Const	47			

Step	Key	Code	Display x	Display y	Display z
0	x←	67			
1	−	34			
2	c	16			
3	x→	23			
4	−	34			
5	6	06			
6	9	11			
7	2	02			
8	FMT	42			
9	GoTo	44			
a	y≷	24			
b	−	34			
c	5	05			
d	2	02			
1 0	2	02			
1	4	04			
2	FMT	42			
3	y→	40			
4	y≷	24			
5	−	34			
6	4	04			
7	2	02			
8	2	02			
9	5	05			
a	FMT	42			
b	y→	40			
c	FMT	42			
d	END	46			

Storage

	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
f																
e																
d																
c																
b																
a																
9																
8																
7																
6																
5																
4																
3																
2																
1																
0																

Title P95-Interpolation Program For Scattering Parameters Data.

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
00	b	14			
01	↑	27			
02	a	13			
03	−	34			
04	c	16			
05	↑	27			
06	d	17			
07	−	34			
08	↓	25			
09	÷	35			
0a	y→	40			
0b	a	13			
0c	b	14			
0d	↑	27			

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
00	a	13			
01	↑	27			
02	c	16			
03	X	36			
04	↓	25			
05	−	34			
06	y→	40			
07	b	14			
08	2	02			
09	4	04			
0a	7	07			
0b	Fit	42			
0c	π	56			
0d	↑	27			

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
00	a	13			
01	X	36			
02	b	14			
03	+	33			
04	y→	40			
05	a	13			
06	Fit	42			
07	END	46			
08					
09					
0a					
0b					
0c					
0d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title ρ41-Zin Computation with Output Terminated By R/S.

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	2	02			
03	9	11			
04	FMT	42			
05	π	56			
06	↑	27			
07	2	02			
08	0	00			
09	6	06			
0a	FMT	42			
0b	π	56			
0c	X→	27			
0d	a	13			
10	÷	35			
11	2	02			
12	2	02			
13	8	10			
14	FMT	42			
15	π	56			
16	↑	27			
17	a	13			
18	÷	35			
19	↓	25			
1a	acct	60			
1b	2	02			
1c	2	02			
1d	7	07			
20	FMT	42			
21	π	56			
22	↑	27			
23	2	02			
24	2	02			
25	6	06			
26	FMT	42			
27	π	56			
28	acct	60			
29	RCL	61			
2a	/acc-	63			
2b	ToRect	66			
2c	ln x	45			
2d	Acct	60			
30	2	02			
31	3	03			
32	3	03			
33	FMT	42			
34	π	56			
35	↑	27			
36	a	13			
37	÷	35			
38	2	02			
39	3	03			
3a	2	02			
3b	FMT	42			
3c	π	56			
3d	↑	27			
40	a	13			
41	÷	35			
42	2	02			
43	3	03			
44	0	00			
45	FMT	42			
46	π	56			
47	+	33			
48	2	02			
49	3	03			
4a	1	01			
4b	FMT	42			
4c	π	56			
4d	Roll↑	22			
50	+	33			
51	↓	25			
52	x≷y	30			
53	ToRect	62			
54	ln x	65			
55	acc-	63			
56	RCL	61			
57	e^x	74			
58	ToRect	66			
59	↑	27			
5a	2	02			
5b	3	03			
5c	4	04			
5d	FMT	42			
60	y→	40			
61	↓	25			
62	2	02			
63	3	03			
64	5	05			
65	FMT	42			
66	y→	40			
67	FMT	42			
68	END	46			

Storage

f	
e	8
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

HEWLETT·PACKARD

Title #42-Computation Of Output Impedance With Input Terminated By R_{in}.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0 0	Clear	20			
1	2	02			
2	2	02			
3	9	11			
4	FMT	42			
5	π	56			
6	↑	27			
7	2	02			
8	0	00			
9	.5	05			
a	FMT	42			
b	π	56			
c	x→	23			
d	a	13			
1 0	÷	35			
1	2	02			
2	2	02			
3	8	10			
4	FMT	42			
5	π	56			
6	↑	27			
7	a	13			
8	÷	35			
9	↓	25			
a	acc+	60			
b	2	02			
c	3	03			
d	3	03			
2 0	FMT	42			
1	π	56			
2	↑	27			
3	2	02			
4	3	03			
5	2	02			
6	FMT	42			
7	π	56			
8	acc+	60			
9	RCL	61			
a	Acc-	63			
b	To Pdat	62			
c	Rnx	65			
d	Rclt	66			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
3 0	2	02			
1	2	02			
2	7	07			
3	FMT	42			
4	π	56			
5	↑	27			
6	a	13			
7	÷	35			
8	2	02			
9	2	02			
a	6	06			
b	FMT	42			
c	π	56			
d	↑	27			
4 0	a	13			
1	÷	35			
2	2	02			
3	3	03			
4	0	00			
5	FMT	42			
6	π	56			
7	+	33			
8	2	02			
9	3	03			
a	1	01			
b	FMT	42			
c	π	56			
d	Rolldt	22			
5 0	+	33			
1	↓	25			
2	x⇄y	30			
3	To Pdat	62			
4	Rnx	65			
5	acc-	63			
6	RCL	61			
7	a	13			
8	To Rclt	66			
9	1	01			
a	2	02			
b	3	03			
c	4	04			
d	FMT	42			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
6 0	y→	40			
1	↓	25			
2	2	02			
3	3	03			
4	5	05			
5	FMT	42			
6	y→	40			
7	FMT	42			
8	END	46			
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P43-Computation Of Insertion Transmission For Given R_s and R_L.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	1	01			
01	9	11			
02	FIX	42			
03	GoTo	44			
04	Clear	20			
05	2	02			
06	3	03			
07	5	05			
08	FIX	42			
09	π	56			
0a	↑	27			
0b	2	02			
0c	3	03			
0d	4	04			
10	FIX	42			
11	π	56			
12	↑	27			
13	2	02			
14	0	00			
15	5	05			
16	FIX	42			
17	π	56			
18	x→	23			
19	a	13			
1a	+	33			
1b	↓	25			
1c	ToPolar	62			
1d	lnx	65			
20	acc-	63			
21	2	02			
22	3	03			
23	3	03			
24	FIX	42			
25	π	56			
26	↑	27			
27	2	02			
28	0	00			
29	6	06			
2a	FIX	42			
2b	π	56			
2c	x→	23			
2d	b	14			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	÷	35			
31	2	02			
32	3	03			
33	1	01			
34	FIX	42			
35	π	56			
36	+	33			
37	2	02			
38	3	03			
39	2	02			
3a	FIX	42			
3b	π	56			
3c	↑	27			
3d	b	14			
40	÷	35			
41	2	02			
42	3	03			
43	0	00			
44	FIX	42			
45	π	56			
46	+	33			
47	↓	25			
48	ToPolar	62			
49	lnX	65			
4a	acc-	63			
4b	Rcl	61			
4c	y→	40			
4d	c	16			
50	e^x	74			
51	↑	27			
52	X	36			
53	4	04			
54	X	36			
55	a	13			
56	X	36			
57	b	14			
58	÷	35			
59	↓	25			
5a	LnX	75			
5b	↑	27			
5c	↓	01			
5d	0	00			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60	X	36			
61	c	16			
62	↑	27			
63	π	56			
64	÷	35			
65	1	01			
66	8	10			
67	0	00			
68	X	36			
69	2	02			
6a	3	03			
6b	7	07			
6c	FIX	42			
6d	y→	40			
70	↓	25			
71	2	02			
72	3	03			
73	6	06			
74	FIX	42			
75	y→	40			
76	FIX	42			
77	END	46			

Storage	
f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P44-Voltage Standing Wave Ratio Calculation.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	1	01			
01	+	04			
02	Fix	42			
03	GoTo	44			
04	2	02			
05	3	03			
06	7	07			
07	Fix	42			
08	π	56			
09	↑	27			
0a	2	02			
0b	3	03			
0c	6	06			
0d	Fix	42			
10	π	56			
11	To Polar	62			
12	Roll↓	31			
13	↓	25			
14	1	01			
15	+	33			
16	Roll↑	22			
17	−	34			
18	↓	25			
19	÷	35			
1a	2	02			
1b	3	03			
1c	6	06			
1d	Fix	42			
20	y→	40			
21	Clear	20			
22	1	02			
23	3	03			
24	7	07			
25	Fix	42			
26	y→	40			
27	Fix	42			
28	End	46			
29					
2a					
2b					
2c					
2d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P45-Reflection Coefficient Calculation.

HEWLETT-PACKARD 67 HEWLETT-PACKARD 97 HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	3	03			
03	5	05			
04	FIX	42			
05	π	56			
06	x→	23			
07	d	17			
08	↑	27			
09	2	02			
0a	3	03			
0b	4	04			
0c	FIX	42			
0d	π	56			
10	x→	23			
11	c	16			
12	↑	27			
13	2	02			
14	0	00			
15	5	05			
16	FIX	42			
17	π	56			
18	x→	23			
19	b	14			
1a	−	34			
1b	↓	25			
1c	Toggle	62			
1d	Inx	65			
20	acct	60			
21	d	17			
22	↑	27			
23	c	16			
24	↑	27			
25	b	14			
26	+	33			
27	↓	25			
28	Toggle	62			
29	Inx	65			
2a	Dsz	63			
2b	acct	60			
2c	R/S	51			
2d	P/R	52			

Step	Key	Code	Display x	Display y	Display z
30	↑	27			
31	2	02			
32	3	03			
33	6	06			
34	FIX	42			
35	y→	40			
36	↓	25			
37	2	02			
38	3	03			
39	7	07			
3a	FIX	42			
3b	y→	40			
3c	FIX	42			
3d	END	46			
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
7a					
7b					
7c					
7d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P46-Sub-routine For Overall Chain Matrix Printout.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0	Clear	20			
1	2	02			
2	4	04			
3	7	07			
4	FIT	42			
5	π	56			
6	x²y	30			
7	Print	45			
8	1	01			
9	1	01			
a	↑	27			
b	2	02			
c	2	02			
d	7	07			
10	FIT	42			
11	π	56			
12	↑	27			
13	2	02			
14	2	02			
15	6	06			
16	FIT	42			
17	π	56			
18	Print	45			
19	1	01			
1a	2	02			
1b	↑	27			
1c	2	02			
1d	2	02			
20	9	11			
21	FIT	42			
22	π	56			
23	↑	27			
24	2	02			
25	2	02			
26	8	10			
27	FIT	42			
28	π	56			
29	Print	45			
2a	2	02			
2b	1	01			
2c	↑	27			
2d	3	03			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	3	03			
31	1	01			
32	FIT	42			
33	π	56			
34	↑	27			
35	2	02			
36	3	03			
37	0	00			
38	FIT	42			
39	π	56			
3a	Print	45			
3b	2	02			
3c	2	02			
3d	↑	27			
40	2	02			
41	3	03			
42	3	03			
43	FIT	42			
44	π	56			
45	↑	27			
46	2	02			
47	3	03			
48	2	02			
49	FIT	42			
4a	π	56			
4b	Print	45			
4c	FMT	42			
4d	END	46			
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P51-Sub-routine For Printing Input Or Output Impedance.

Step	Key	Code	Display x	Display y	Display z
0	2	02			
1	4	04			
2	7	07			
3	FMT	42			
4	π	56			
5	↑	27			
6	2	02			
7	3	03			
8	5	05			
9	FMT	42			
a	π	56			
b	↑	27			
c	2	02			
d	3	03			
10	4	04			
1	FMT	42			
2	π	56			
3	Print	45			
4	FMT	42			
5	END	46			
6					
7					
8					
9					
a					
b					
c					
d					
20					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
10					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
20					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
10					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

HEWLETT-PACKARD

Title P52-Sub-routine For Printing Frequency Response Data.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	4	04			
02	7	07			
03	FMT	42			
04	π	56			
05	↑	27			
06	2	02			
07	3	03			
08	7	07			
09	FMT	42			
0a	π	56			
0b	↑	27			
0c	2	02			
0d	3	03			
10	6	06			
11	FMT	42			
12	π	56			
13	Print	45			
14	FMT	42			
15	END	46			
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
7a					
7b					
7c					
7d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P53-Polar Plot For Reflection Coefficient (Smith-Chart Presentatio

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0 0	4	04			
1	5	05			
2	FMT	42			
3	GoTo	44			
4	2	02			
5	0	00			
6	2	02			
7	FMT	42			
8	π	56			
9	X→	23			
a	d	17			
b	2	02			
c	3	03			
d	7	07			
1 0	FMT	42			
1	π	56			
2	↑	27			
3	d	17			
4	X	36			
5	2	02			
6	5	05			
7	0	00			
8	X	36			
9	2	02			
a	3	03			
b	6	06			
c	FMT	42			
d	π	56			
2 0	↑	27			
1	d	17			
2	X	36			
3	2	02			
4	5	05			
5	0	00			
6	X	36			
7	↑	27			
8	FMT	42			
9	↑	27			
a	FMT	42			
b	END	44			
c					
d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
1 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
2 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P54-Sub-routine For Frequency Response Plot On Linear Scale.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	4	04			
02	7	07			
03	FMT	42			
04	π	56			
05	↑	27			
06	1	01			
07	9	11			
08	9	11			
09	FMT	42			
0a	π	56			
0b	−	34			
0c	2	02			
0d	0	00			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
10	0	00			
11	FMT	42			
12	π	56			
13	÷	35			
14	5	05			
15	0	00			
16	0	00			
17	X	36			
18	x↔	40			
19	a	12			
1a	2	02			
1b	3	03			
1c	6	06			
1d	FMT	42			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
20	π	56			
21	↑	27			
22	2	02			
23	0	00			
24	1	01			
25	FMT	42			
26	π	56			
27	−	34			
28	2	02			
29	0	00			
2a	2	02			
2b	FMT	42			
2c	π	56			
2d	÷	35			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	5	05			
31	0	00			
32	0	00			
33	X	36			
34	a	13			
35	FMT	42			
36	↓	25			
37	FMT	42			
38	END	46			
39					
3a					
3b					
3c					
3d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

APPENDIX II

TIME DOMAIN CIRCUIT ANALYSIS PROGRAM

PROGRAMMING STEPS

Title PO-Time Domain Circuit Analysis Input Program.

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	1	01			
02	↑	27			
03	1	01			
04	0	00			
05	9	11			
06	acc+	60			
07	1	01			
08	STOP	41			
09	↑	27			
0a	2	02			
0b	4	04			
0c	7	07			
0d	FMT	42			
10	y→	40			
11	1	01			
12	x→	23			
13	d	17			
14	e	12			
15	↑	27			
16	↑	27			
17	STOP	41			
18	↑	27			
19	1	01			
1a	0	00			
1b	X	36			
1c	↓	25			
1d	+	33			
20	f	15			
21	FMT	42			
22	y→	40			
23	RCL	61			
24	FMT	42			
25	TT	56			
26	↑	27			
27	d	17			
28	STOP	41			
29	↑	27			
2a	f	15			
2b	f	27			
2c	d	17			
2d	−	34			
30	Roll↓	31			
31	FMT	42			
32	y→	40			
33	Roll↓	31			
34	3	03			
35	x≷y	50			
36	4	04			
37	1	01			
38	1	01			
39	+	33			
3a	y→	40			
3b	d	17			
3c	GoTo	44			
3d	2	02			
40	3	03			
41	RCL	61			
42	2	02			
43	4	04			
44	7	07			
45	FMT	42			
46	TT	56			
47	x≷y	50			
48	5	05			
49	4	04			
4a	1	01			
4b	↑	27			
4c	4	04			
4d	Cpn,Spn	32			
50	acc+	60			
51	GoTo	44			
52	1	01			
53	1	01			
54	Clear	20			
55	2	02			
56	↑	27			
57	STOP	41			
58	↑	27			
59	2	02			
5a	4	04			
5b	5	05			
5c	FMT	42			
5d	y→	40			
60	↓	25			
61	2	02			
62	4	04			
63	4	04			
64	FMT	42			
65	y→	40			
66	END	46			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P1-Time Domain Circuit Analysis Initialization Program.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	1	01			
02	1	01			
03	1	01			
04	FMT	42			
05	X	36			
06	↑	27			
07	1	01			
08	8	10			
09	9	11			
0a	x≷y	50			
0b	1	01			
0c	5	05			
0d	1	01			
10	+	33			
11	↓	25			
12	GoTo	44			
13	0	00			
14	4	04			
15	1	01			
16	↑	27			
17	1	01			
18	1	01			
19	0	00			
1a	FMT	42			
1b	y→	40			
1c	1	01			
1d	2	02			
20	0	00			
21	FMT	42			
22	y→	40			
23	1	01			
24	4	04			
25	0	00			
26	FMT	42			
27	y→	40			
28	1	01			
29	6	06			
2a	0	00			
2b	FMT	42			
2c	y→	40			
2d	1	01			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	7	07			
31	0	00			
32	FMT	42			
33	y→	40			
34	1	01			
35	8	10			
36	0	00			
37	FMT	42			
38	y→	40			
39	2	02			
3a	4	04			
3b	4	04			
3c	FMT	42			
3d	π	56			
40	↑	27			
41	1	01			
42	3	03			
43	0	00			
44	FMT	42			
45	y→	40			
46	1	01			
47	0	00			
48	9	11			
49	↑	27			
4a	2	02			
4b	4	04			
4c	6	06			
4d	FMT	42			
50	y→	40			
51	2	02			
52	4	04			
53	6	06			
54	FMT	42			
55	π	56			
56	FMT	42			
57	π	56			
58	FMT	42			
59	GoTo	44			
5a	2	02			
5b	FMT	42			
5c	GoTo	44			
5d	2	02			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60	4	04			
61	7	07			
62	FMT	42			
63	π	56			
64	↑	27			
65	1	01			
66	1	01			
67	3	03			
68	↑	27			
69	2	02			
6a	4	04			
6b	6	06			
6c	FMT	42			
6d	π	56			
70	−	34			
71	4	04			
72	÷	35			
73	↓	25			
74	Pause	57			
75	Pause	57			
76	x≷y	50			
77	8	10			
78	5	05			
79	4	04			
7a	↑	27			
7b	2	02			
7c	4	04			
7d	6	06			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P1-Continue.

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
8 0	FMT	42			
1	—	34			
2	GoTo	44			
3	5	05			
4	1	01			
5	8	10			
6	FMT	42			
7	GoTo	44			
8	2	02			
9	4	04			
a	5	05			
b	FMT	42			
c	π	56			
d	↑	27			
9 0	1	01			
1	9	11			
2	4	04			
3	FMT	42			
4	÷	35			
5	2	02			
6	4	04			
7	6	06			
8	FMT	42			
9	π	56			
a	↑	27			
b	FMT	42			
c	π	56			
d	↑	27			
a 0	2	02			
1	4	04			
2	1	01			
3	FMT	42			
4	y→	40			
5	2	02			
6	9	11			
7	Roll	22			
8	FMT	42			
9	y→	40			
a	2	02			
b	FMT	42			
c	GoTo	44			
d	∞	02			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
b 0	4	04			
1	1	01			
2	FMT	42			
3	π	56			
4	↑	27			
5	2	02			
6	4	04			
7	6	06			
8	FMT	42			
9	π	56			
a	FMT	42			
b	y→	40			
c	END	46			
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P2-Polynomial Matrix Multiplication.

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	4	04			
02	6	06			
03	FMT	42			
04	π	56			
05	FMT	42			
06	π	56			
07	↑	27			
08	2	02			
09	0	00			
0a	x↔y	30			
0b	x≷y	52			
0c	3	03			
0d	5	05			
10	1	01			
11	3	03			
12	0	00			
13	X→	23			
14	−	34			
15	9	11			
16	1	01			
17	1	01			
18	0	00			
19	X→	23			
1a	−	34			
1b	8	10			
1c	3	03			
1d	FMT	42			
20	GoTo	44			
21	1	01			
22	7	07			
23	0	00			
24	X→	23			
25	−	34			
26	9	11			
27	1	01			
28	5	05			
29	0	00			
2a	X→	23			
2b	−	34			
2c	8	10			
2d	3	03			
30	FMT	42			
31	GoTo	44			
32	GoTo	44			
33	5	05			
34	7	07			
35	1	01			
36	1	01			
37	0	00			
38	X→	23			
39	−	34			
3a	9	11			
3b	1	01			
3c	3	03			
3d	0	00			
40	X→	23			
41	−	34			
42	8	10			
43	3	03			
44	FMT	42			
45	GoTo	44			
46	1	01			
47	5	05			
48	0	00			
49	X→	23			
4a	−	34			
4b	9	11			
4c	1	01			
4d	7	07			
50	0	00			
51	X→	23			
52	−	34			
53	8	10			
54	3	03			
55	FMT	42			
56	GoTo	44			
57	FMT	42			
58	END	46			
59					
5a					
5b					
5c					
5d					
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f
e
d
c
b
a
9
8
7
6
5
4
3
2
1
0

HEWLETT·PACKARD

Title P3-Polynomial Functions Manupilation For P2.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
0	x←	67			
1	−	34			
2	9	11			
3	x→	23			
4	−	34			
5	℮	12			
6	2	02			
7	1	01			
8	0	00			
9	x→	23			
a	−	34			
b	f	15			
c	9	11			
d	x→	23			
1					
0	−	34			
1	d	17			
2	9	11			
3	1	01			
4	FMT	42			
5	GoTo	44			
6	1	01			
7	9	11			
8	4	04			
9	x→	23			
a	−	34			
b	℮	12			
c	2	02			
d	2	02			
2					
0	0	00			
1	x→	23			
2	−	34			
3	f	15			
4	2	02			
5	x→	23			
6	−	34			
7	d	17			
8	9	11			
9	1	01			
a	FMT	42			
b	GoTo	44			
c	9	11			
d	0	00			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
3					
0	FMT	42	-		
1	GoTo	44			
2	x←	67			
3	−	34			
4	8	10			
5	f	27			
6	1	01			
7	0	00			
8	+	33			
9	y→	40			
a	−	34			
b	℮	12			
c	2	02			
d	2	02			
4					
0	0	00			
1	x→	23			
2	−	34			
3	f	15			
4	9	11			
5	x→	23			
6	−	34			
7	d	17			
8	9	11			
9	1	01			
a	FMT	42			
b	GoTo	44			
c	9	11			
d	0	00			
5					
0	FMT	42			
1	GoTo	44			
2	2	02			
3	3	03			
4	0	00			
5	x→	23			
6	−	34			
7	℮	12			
8	2	02			
9	0	00			
a	0	00			
b	x→	23			
c	−	34			
d	f	15			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
6					
0	9	11			
1	1	01			
2	FMT	42			
3	GoTo	44			
4	x←	67			
5	−	34			
6	9	11			
7	f	27			
8	1	01			
9	0	00			
a	+	33			
b	y→	40			
c	−	34			
d	℮	12			
7					
0	2	02			
1	1	01			
2	0	00			
3	x→	23			
4	−	34			
5	f	15			
6	9	11			
7	1	01			
8	FMT	42			
9	GoTo	44			
a	1	01			
b	9	11			
c	7	07			
d	x→	23			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P3-Continue.

Step	Key	Code	Display x	Display y	Display z
8 0	−	34			
1	a	12			
2	2	02			
3	2	02			
4	0	00			
5	x→	23			
6	−	34			
7	f	15			
8	2	02			
9	x→	23			
a	−	34			
b	d	17			
c	9	11			
d	1	01			
9 0	FMT	42			
1	GoTo	44			
2	9	11			
3	0	00			
4	FMT	42			
5	GoTo	44			
6	X←	67			
7	−	34			
8	8	10			
9	↑	27			
a	1	01			
b	0	00			
c	+	33			
d	y→	40			
a 0	−	34			
1	a	12			
2	2	02			
3	2	02			
4	0	00			
5	x→	23			
6	−	34			
7	1	15			
8	9	11			
9	x→	23			
a	−	34			
b	d	17			
c	9	11			
d	1	01			

Step	Key	Code	Display x	Display y	Display z
b 0	FMT	42			
1	GoTo	44			
2	2	02			
3	1	01			
4	0	00			
5	x→	23			
6	−	34			
7	a	12			
8	x←	67			
9	−	34			
a	8	10			
b	↑	27			
c	1	01			
d	0	00			
c 0	+	33			
1	y→	40			
2	−	34			
3	f	15			
4	9	11			
5	1	01			
6	FMT	42			
7	GoTo	44			
8	9	11			
9	0	00			
a	FMT	42			
b	GoTo	44			
c	X←	67			
d	−	34			
d 0	8	10			
1	↑	27			
2	1	01			
3	0	00			
4	+	33			
5	y→	40			
6	−	34			
7	a	12			
8	4	04			
9	FMT	42			
a	GoTo	44			
b	FMT	42			
c	END	46			
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage	
f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

HEWLETT·PACKARD

Title P4-Continuation Of P3.

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	2	02			
02	0	00			
03	x→	23			
04	−	34			
05	f	15			
06	9	11			
07	1	01			
08	FMT	42			
09	GoTo	44			
0a	2	02			
0b	1	01			
0c	0	00			
0d	x→	23			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
10	−	34			
11	e	12			
12	x←	67			
13	−	34			
14	8	10			
15	↑	27			
16	1	01			
17	0	00			
18	+	33			
19	y→	40			
1a	−	34			
1b	f	15			
1c	9	11			
1d	1	01			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
20	FMT	42			
21	GoTo	44			
22	x←	67			
23	−	34			
24	8	10			
25	x→	23			
26	−	34			
27	e	12			
28	2	02			
29	1	01			
2a	0	00			
2b	x→	23			
2c	−	34			
2d	f	15			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
30	9	11			
31	1	01			
32	FMT	42			
33	GoTo	44			
34	9	11			
35	0	00			
36	FMT	42			
37	GoTo	44			
38	2	02			
39	0	00			
3a	0	00			
3b	x→	23			
3c	−	34			
3d	e	12			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
40	2	02			
41	2	02			
42	0	00			
43	x→	23			
44	−	34			
45	f	15			
46	9	11			
47	1	01			
48	FMT	42			
49	GoTo	44			
4a	9	11			
4b	3	03			
4c	FMT	42			
4d	GoTo	44			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
50	e	02			
51	3	03			
52	0	00			
53	x→	23			
54	−	34			
55	e	12			
56	x←	67			
57	−	34			
58	8	10			
59	x→	23			
5a	−	34			
5b	f	15			
5c	9	11			
5d	1	01			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
60	FMT	42			
61	GoTo	44			
62	x←	67			
63	−	34			
64	8	10			
65	x→	23			
66	−	34			
67	7	07			
68	9	11			
69	4	04			
6a	FMT	42			
6b	GoTo	44			
6c	FMT	42			
6d	END	46			

70					
71					
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7a					
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Storage

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Title P8-Unity Matrix.

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	1	01			
02	9	11			
03	5	05			
04	FIX	42			
05	X	36			
06	1	27			
07	1	01			
08	9	11			
09	9	11			
0a	x≠y	50			
0b	1	01			
0c	5	05			
0d	1	01			
10	+	33			
11	1	25			
12	GoTo	44			
13	0	00			
14	4	04			
15	1	01			
16	↑	27			
17	1	01			
18	9	11			
19	4	04			
1a	FIX	42			
1b	y→	40			
1c	1	01			
1d	9	11			
20	7	07			
21	FIX	42			
22	y→	40			
23	FIX	42			
24	END	46			
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					

Step	Key	Code	Display x	Display y	Display z
30					
31					
32					
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35					
36					
37					
38					
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3a					
3b					
3c					
3d					
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4a					
4b					
4c					
4d					
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51					
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56					
57					
58					
59					
5a					
5b					
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					
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7a					
7b					
7c					
7d					

Storage

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Title P90-Polynomial Multiplication.

HEWLETT·PACKARD [97]

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	3	03			
03	0	00			
04	acct	60			
05	f	15			
06	FMT	42			
07	X	36			
08	↑	27			
09	2	02			
0a	3	03			
0b	9	11			
0c	x≷y	50			
0d	1	01			
10	7	07			
11	0	00			
12	↑	27			
13	1	01			
14	GoTo	44			
15	0	00			
16	4	04			
17	Clear	20			
18	2	02			
19	1	01			
1a	0	00			
1b	↑	27			
1c	e	12			
1d	+	33			
20	↓	25			
21	FMT	42			
22	π	56			
23	↑	27			
24	2	02			
25	2	02			
26	0	00			
27	↑	27			
28	6	15			
29	+	33			
2a	↓	25			
2b	FMT	42			
2c	π	56			
2d	X	36			

HEWLETT·PACKARD [97]

Step	Key	Code	Display x	Display y	Display z
30	↑	27			
31	RCL	61			
32	+	33			
33	9	11			
34	•	21			
35	1	01			
36	x≷y	52			
37	4	04			
38	2	02			
39	2	02			
3a	3	03			
3b	0	00			
3c	+	33			
3d	↓	25			
40	FMT	42			
41	+	33			
42	f	15			
43	↑	27			
44	9	11			
45	x≷y	50			
46	5	05			
47	1	01			
48	0	00			
49	↑	27			
4a	1	01			
4b	acct	60			
4c	GoTo	44			
4d	1	01			
50	B	10			
51	e	12			
52	↑	27			
53	9	11			
54	x≷y	50			
55	6	06			
56	2	02			
57	1	01			
58	↑	27			
59	0	00			
5a	x→	23			
5b	f	15			
5c	acct	60			
5d	GoTo	44			

HEWLETT·PACKARD [97]

Step	Key	Code	Display x	Display y	Display z
60	1	01			
61	B	10			
62	2	02			
63	3	03			
64	0	00			
65	x→	23			
66	−	34			
67	e	12			
68	2	02			
69	1	01			
6a	0	00			
6b	x→	23			
6c	−	34			
6d	f	15			
70	9	11			
71	x→	23			
72	−	34			
73	d	17			
74	9	11			
75	1	01			
76	FMT	42			
77	GoTo	44			
78	FMT	42			
79	END	46			
7a					
7b					
7c					
7d					

Storage

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Title P91-Data Transfer Program.

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
00	clear	20			
01	x←	67			
02	−	34			
03	e	12			
04	↑	27			
05	x←	67			
06	−	34			
07	f	15			
08	acc+	60			
09	x←	67			
0a	−	34			
0b	d	17			
0c	+	33			
0d	y→	40			
10	d	17			
11	e	12			
12	FMT	42			
13	π	56			
14	↑	27			
15	f	15			
16	FMT	42			
17	y→	40			
18	e	12			
19	↑	27			
1a	d	17			
1b	x^2y	50			
1c	2	02			
1d	6	06			
20	1	01			
21	↑	27			
22	acc+	60			
23	GoTo	44			
24	1	01			
25	1	01			
26	x←	67			
27	−	34			
28	d	17			
29	↑	27			
2a	9	11			
2b	x^2y	50			
2c	4	04			
2d	5	05			

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
30	0	00			
31	↑	27			
32	1	01			
33	acc+	60			
34	f	15			
35	FMT	42			
36	x	36			
37	1	01			
38	↑	27			
39	x←	67			
3a	−	34			
3b	d	17			
3c	+	33			
3d	y→	40			
40	−	34			
41	d	17			
42	GoTo	44			
43	2	02			
44	6	06			
45	FMT	42			
46	END	46			
47					
48					
49					
4a					
4b					
4c					
4d					
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51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
0					
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2					
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4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

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P92-Detection Of Degree Of Polynomial Function.

Title P93-Polynomial Addition.

Step	P92 Key	Code	Display x	Display y	Display z	Step	P93 Key	Code	Display x	Display y	Display z	Step	Key	Code	Display x	Display y	Display z
00	Clear	20				00	Clear	20				0					
01	x←	67				01	2	02				1					
02	−	34				02	1	01				2					
03	e	12				03	0	00				3					
04	↑	27				04	↑	27				4					
05	9	11				05	2	02				5					
06	+	33				06	2	02				6					
07	x⇄y	30				07	0	00				7					
08	acc+	60				08	acc+	60				8					
09	0	00				09	↓	15				9					
0a	↑	27				0a	FMT	42				a					
0b	↓	15				0b	π	56				b					
0c	FMT	42				0c	↑	27				c					
0d	π	56				0d	e	12				d					
10	x²−y	50				10	FMT	42				0					
11	1	01				11	+	33				1					
12	d	17				12	FMT	42				2					
13	e	12				13	π	56				3					
14	↑	27				14	↑	27				4					
15	2	02				15	↓	15				5					
16	4	04				16	↑	27				6					
17	0	02				17	1	01				7					
18	FMT	42				18	0	00				8					
19	y→	40				19	+	33				9					
1a	GoTo	44				1a	↓	25				a					
1b	2	02				1b	FMT	42				b					
1c	b	14				1c	y→	40				c					
1d	0	00				1d	↓	15				d					
20	↑	27				20	↑	27									
21	e	12				21	2	02									
22	x²y	52				22	2	02									
23	1	01				23	9	11									
24	3	03				24	x²y	50									
25	1	01				25	2	02									
26	a=0?	34				26	C	16									
27	↑	27				27	1	01									
28	GoTo	44				28	↑	27									
29	0	00				29	GoTo	44									
2a	8	10				2a	0	00									
2b	FMT	42				2b	8	10									
2c	END	46				2c	FMT	42									
2d						2d	END	46									

Storage

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HEWLETT-PACKARD

Title P94-Common Factor In "S" Cancellation Of Polynomial Function N

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	X←	67			
02	−	34			
03	7	07			
04	acct	60			
05	0	00			
06	↑	27			
07	f	15			
08	FMT	42			
09	π	56			
0a	$x^2_{<y}$	50			
0b	1	01			
0c	9	11			
0d	e	12			
10	↑	27			
11	2	02			
12	4	04			
13	2	02			
14	FMT	42			
15	y→	40			
16	GoTo	44			
17	2	02			
18	9	11			
19	9	11			
1a	↑	27			
1b	e	12			
1c	$x^2_{<y}$	52			
1d	e	02			
20	4	04			
21	GoTo	44			
22	0	00			
23	d	17			
24	1	01			
25	↑	27			
26	GoTo	44			
27	0	00			
28	4	04			
29	Clear	20			
2a	X←	67			
2b	−	34			
2c	7	07			
2d	↑	27			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	1	01			
31	0	00			
32	+	33			
33	↑	25			
34	acct	60			
35	0	00			
36	↑	27			
37	f	15			
38	FMT	42			
39	π	56			
3a	$x^2_{<y}$	50			
3b	4	04			
3c	9	11			
3d	e	12			
40	↑	27			
41	2	02			
42	4	04			
43	3	03			
44	FMT	42			
45	y→	40			
46	GoTo	44			
47	5	05			
48	9	11			
49	9	11			
4a	↑	27			
4b	e	12			
4c	$x^2_{<y}$	52			
4d	5	05			
50	4	04			
51	GoTo	44			
52	3	03			
53	d	17			
54	1	01			
55	↑	27			
56	GoTo	44			
57	3	03			
58	4	04			
59	FMT	42			
5a	END	46			
5b					
5c					
5d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					
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76					
77					
78					
79					
7a					
7b					
7c					
7d					

Storage

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Title P95-Detection Of The Lowest Degree In Polynomial Function.

HEWLETT-PACKARD [95]

Step	Key	Code	Display x	Display y	Display z
00	9	11			
01	5	05			
02	FMT	42			
03	GoTo	44			
04	Clear	20			
05	x←	67			
06	−	34			
07	7	07			
08	↑	27			
09	9	11			
0a	+	33			
0b	y→	40			
0c	d	17			
0d	1	01			

HEWLETT-PACKARD [95]

Step	Key	Code	Display x	Display y	Display z
10	0	00			
11	+	33			
12	y→	40			
13	c	16			
14	2	02			
15	4	04			
16	2	02			
17	FMT	42			
18	π	56			
19	↑	27			
1a	2	02			
1b	4	04			
1c	3	03			
1d	FMT	42			

HEWLETT-PACKARD [95]

Step	Key	Code	Display x	Display y	Display z
20	π	56			
21	x≷y	53			
22	2	02			
23	5	05			
24	x≷y	30			
25	x←	67			
26	−	34			
27	7	07			
28	acct	60			
29	RCL	61			
2a	+	33			
2b	x≷y	30			
2c	FMT	42			
2d	π	56			

HEWLETT-PACKARD [95]

Step	Key	Code	Display x	Display y	Display z
30	x≷y	30			
31	FMT	42			
32	y→	40			
33	RCL	61			
34	+	33			
35	d	17			
36	x≷y	50			
37	4	04			
38	1	01			
39	0	00			
3a	↑	27			
3b	1	01			
3c	GoTo	44			
3d	2	02			

HEWLETT-PACKARD [95]

Step	Key	Code	Display x	Display y	Display z
40	8	10			
41	1	01			
42	+	33			
43	e	12			
44	−	34			
45	y→	40			
46	b	14			
47	b	14			
48	↑	27			
49	d	17			
4a	x≷y	52			
4b	5	05			
4c	c	16			
4d	0	00			

HEWLETT-PACKARD [95]

Step	Key	Code	Display x	Display y	Display z
50	↑	27			
51	b	14			
52	FMT	42			
53	X	36			
54	↑	27			
55	1	01			
56	+	33			
57	y→	40			
58	b	14			
59	GTo	44			
5a	4	04			
5b	7	07			
5c	d	17			
5d	↑	27			

HEWLETT-PACKARD [95]

Step	Key	Code	Display x	Display y	Display z
60	c	16			
61	x≷y	50			
62	7	07			
63	6	06			
64	x→	23			
65	d	17			
66	1	01			
67	0	00			
68	↑	27			
69	x←	67			
6a	−	34			
6b	7	07			
6c	+	33			
6d	y→	40			

HEWLETT-PACKARD [95]

Step	Key	Code	Display x	Display y	Display z
70	−	34			
71	7	07			
72	Clear	20			
73	GoTo	44			
74	1	01			
75	4	04			
76	FMT	42			
77	END	46			
78					
79					
7a					
7b					
7c					
7d					

Storage

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Title P14-Series Connected Parallel R-L-C.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	8	10			
01	FMT	42			
02	GoTo	44			
03	Clear	20			
04	2	02			
05	4	04			
06	6	06			
07	FMT	42			
08	π	56			
09	↑	27			
0a	acc+	60			
0b	1	01			
0c	↑	27			
0d	3	03			
10	acc−	63			
11	RCL	61			
12	FMT	42			
13	π	56			
14	x⇄y	30			
15	FMT	42			
16	π	56			
17	y→	40			
18	a	13			
19	X	36			
1a	↑	27			
1b	1	01			
1c	9	11			
1d	4	04			
20	FMT	42			
21	y→	40			
22	↓	25			
23	1	01			
24	9	11			
25	8	10			
26	FMT	A2			
27	y→	40			
28	1	01			
29	acc+	60			
2a	RCL	61			
2b	FMT	42			
2c	π	56			
2d	↑	27			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	1	01			
31	9	11			
32	5	05			
33	FMT	42			
34	y→	40			
35	a	13			
36	X	36			
37	1	01			
38	9	11			
39	9	11			
3a	FMT	42			
3b	y→	40			
3c	FMT	42			
3d	END	46			
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
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17					
18					
19					
1a					
1b					
1c					
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27					
28					
29					
2a					
2b					
2c					
2d					

Storage	
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1	
0	

Title P15-Series Connected Series R-L-C.

Step	Key	Code	Display x	Display y	Display z
00	8	10			
01	FMT	42			
02	GoTo	44			
03	Clear	20			
04	1	01			
05	9	11			
06	7	07			
07	FMT	42			
08	y→	40			
09	2	02			
0a	4	04			
0b	6	06			
0c	FMT	42			
0d	π	56			
10	↑	27			
11	acc+	60			
12	3	03			
13	↑	27			
14	1	01			
15	acc-	63			
16	Rcl	61			
17	FMT	42			
18	π	56			
19	x⇄y	30			
1a	FMT	42			
1b	π	56			
1c	x→	23			
1d	a	13			
20	X	36			
21	↑	27			
22	1	01			
23	9	11			
24	8	10			
25	FMT	42			
26	y→	40			
27	↓	25			
28	1	01			
29	9	11			
2a	5	05			
2b	FMT	42			
2c	y→	40			
2d	↓	01			
30	acc-	63			
31	Rcl	61			
32	FMT	42			
33	π	56			
34	↑	27			
35	a	13			
36	X	36			
37	1	01			
38	9	11			
39	6	06			
3a	FMT	42			
3b	y→	40			
3c	FMT	42			
3d	END	46			
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Step	Key	Code	Display x	Display y	Display z
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
7a					
7b					
7c					
7d					

Storage

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HEWLETT-PACKARD

Title P24-Shunt Connected Parallel R-L-C.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0 0	8	10			
1	FMT	42			
2	GoTo	44			
3	Clear	20			
4	2	02			
5	4	04			
6	6	06			
7	FMT	42			
8	π	56			
9	↑	27			
a	acc+	60			
b	1	01			
c	↑	27			
d	3	03			
1 0	acc-	63			
1	Rcl	61			
2	FMT	42			
3	π	56			
4	X⇆Y	30			
5	FMT	42			
6	π	56			
7	y→	40			
8	a	13			
9	X	36			
a	↑	27			
b	1	01			
c	9	11			
d	7	07			
2 0	FMT	42			
1	y→	40			
2	↑	25			
3	1	01			
4	9	11			
5	5	05			
6	FMT	42			
7	y→	40			
8	1	01			
9	acc+	60			
a	Rcl	61			
b	FMT	42			
c	π	56			
d	↑	27			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
3 0	1	01			
1	9	11			
2	8	10			
3	FMT	42			
4	y→	40			
5	a	13			
6	X	36			
7	1	01			
8	9	11			
9	6	06			
a	FMT	42			
b	y→	40			
c	FMT	42			
d	END	46			
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P25-Shunt Connected Series R-L-C.

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
00	8	10			
01	FMT	42			
02	GoTo	44			
03	Clear	20			
04	1	01			
05	9	11			
06	4	04			
07	FMT	42			
08	y→	40			
09	2	02			
0a	4	04			
0b	6	06			
0c	FMT	42			
0d	π	56			
10	↑	27			
11	acc+	60			
12	3	03			
13	↑	27			
14	1	01			
15	acc-	63			
16	RCL	61			
17	FMT	42			
18	π	56			
19	x⇄y	30			
1a	FMT	42			
1b	π	56			
1c	x→	23			
1d	a	13			
20	X	36			
21	↑	27			
22	1	01			
23	9	11			
24	5	05			
25	FMT	42			
26	y→	40			
27	↓	25			
28	1	01			
29	9	11			
2a	8	10			
2b	FMT	42			
2c	y→	40			
2d	1	01			

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
30	acc-	63			
31	RCL	61			
32	FMT	42			
33	π	56			
34	↑	27			
35	a	13			
36	X	36			
37	1	01			
38	9	11			
39	9	11			
3a	FMT	42			
3b	y→	40			
3c	FMT	42			
3d	END	46			
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
6a					
6b					
6c					
6d					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
7a					
7b					
7c					
7d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P5-System Function Specification Program.

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	3	03			
02	↑	27			
03	STOP	41			
04	↑	27			
05	2	02			
06	4	04			
07	0	00			
08	FMT	42			
09	y→	40			
0a	Clear	20			
0b	4	04			
0c	↑	27			
0d	STOP	41			
10	↑	27			
11	1	01			
12	0	00			
13	5	05			
14	FMT	42			
15	y→	40			
16	1	01			
17	.	21			
18	5	05			
19	x≷y	53			
1a	4	04			
1b	4	04			
1c	1	01			
1d	↑	27			
20	4	04			
21	↑	27			
22	STOP	41			
23	↑	27			
24	1	01			
25	0	00			
26	7	07			
27	FMT	42			
28	y→	40			
29	↓	25			
2a	1	01			
2b	0	00			
2c	6	06			
2d	FMT	42			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
30	y→	40			
31	2	02			
32	↑	27			
33	4	04			
34	↑	27			
35	STOP	41			
36	↑	27			
37	1	01			
38	0	00			
39	9	11			
3a	FMT	42			
3b	y→	40			
3c	↓	25			
3d	1	01			
40	0	00			
41	B	10			
42	FMT	42			
43	y→	40			
44	Clear	20			
45	5	05			
46	↑	27			
47	STOP	41			
48	↑	27			
49	2	02			
4a	4	04			
4b	7	07			
4c	FMT	42			
4d	y→	40			
50	↓	25			
51	2	02			
52	4	04			
53	5	05			
54	FMT	42			
55	y→	40			
56	B	10			
57	0	00			
58	↑	27			
59	2	02			
5a	4	04			
5b	0	00			
5c	FMT	42			
5d	π	56			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
60	+	33			
61	↓	25			
62	FMT	42			
63	GoTo	44			
64	1	01			
65	9	11			
66	0	00			
67	x→	23			
68	−	34			
69	2	12			
6a	x→	23			
6b	−	34			
6c	7	07			
6d	CONT	47			
70	CONT	47			
71	9	11			
72	4	04			
73	FMT	42			
74	GoTo	44			
75	9	11			
76	2	02			
77	FMT	42			
78	GoTo	44			
79	2	02			
7a	4	04			
7b	0	00			
7c	FMT	42			
7d	π	56			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P5-Continue.

HEWLETT·PACKARD 97

Step	Key	Code	Display x	Display y	Display z
80	↑	27			
81	2	02			
82	4	04			
83	4	04			
84	FMT	42			
85	y→	40			
86	2	02			
87	0	00			
88	0	00			
89	x→	23			
8a	−	34			
8b	R	12			
8c	9	11			
8d	2	02			
90	FMT	42			
91	GoTo	44			
92	2	02			
93	4	04			
94	0	00			
95	FMT	42			
96	π	56			
97	↑	27			
98	2	02			
99	4	04			
9a	3	03			
9b	FMT	42			
9c	y→	40			
9d	END	46			

HEWLETT·PACKARD 98

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					

HEWLETT·PACKARD 67

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					

HEWLETT·PACKARD 67

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P81-Input Impedance Function, Z_{in}.

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
00	1	01			
01	1	01			
02	0	00			
03	X→	23			
04	−	34			
05	e	12			
06	2	02			
07	1	01			
08	0	00			
09	X→	23			
0a	−	34			
0b	f	15			
0c	9	11			
0d	X→	23			
10	−	34			
11	d	17			
12	9	11			
13	1	01			
14	FIX	42			
15	GoTo	44			
16	1	01			
17	6	06			
18	0	00			
19	X→	23			
1a	−	34			
1b	e	12			
1c	2	02			
1d	2	02			
20	0	00			
21	X→	23			
22	−	34			
23	f	15			
24	9	11			
25	X→	23			
26	−	34			
27	d	17			
28	9	11			
29	1	01			
2a	FIX	42			
2b	GoTo	44			
2c	9	11			
2d	0	00			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
30	FIX	42			
31	GoTo	44			
32	2	02			
33	3	03			
34	0	00			
35	X→	23			
36	−	34			
37	e	12			
38	1	01			
39	9	11			
3a	0	00			
3b	X→	23			
3c	−	34			
3d	f	15			
40	9	11			
41	X→	23			
42	−	34			
43	d	17			
44	9	11			
45	1	01			
46	FIX	42			
47	GoTo	44			
48	1	01			
49	2	02			
4a	0	00			
4b	X→	23			
4c	−	34			
4d	e	12			
50	2	02			
51	1	01			
52	0	00			
53	X→	23			
54	−	34			
55	f	15			
56	9	11			
57	X→	23			
58	−	34			
59	d	17			
5a	9	11			
5b	1	01			
5c	FIX	42			
5d	GoTo	44			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
60	1	01			
61	5	05			
62	0	00			
63	X→	23			
64	−	34			
65	e	12			
66	2	02			
67	2	02			
68	0	00			
69	X→	23			
6a	−	34			
6b	f	15			
6c	9	11			
6d	X→	23			
70	−	34			
71	d	17			
72	9	11			
73	1	01			
74	FIX	42			
75	GoTo	44			
76	9	11			
77	0	00			
78	FIX	42			
79	GoTo	44			
7a	2	02			
7b	3	03			
7c	0	00			
7d	X→	23			

Storage	
f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P81-Continue.

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
80	−	34			
81	a	12			
82	2	02			
83	0	00			
84	0	00			
85	x→	23			
86	−	34			
87	t	15			
88	9	11			
89	x→	23			
8a	−	34			
8b	d	17			
8c	9	11			
8d	1	01			
90	FMT	42			
91	GoTo	44			
92	FMT	42			
93	END	46			
94					
95					
96					
97					
98					
99					
9a					
9b					
9c					
9d					
a0					
a1					
a2					
a3					
a4					
a5					
a6					
a7					
a8					
a9					
aa					
ab					
ac					
ad					
b0					
b1					
b2					
b3					
b4					
b5					
b6					
b7					
b8					
b9					
ba					
bb					
bc					
bd					

Step	Key	Code	Display x	Display y	Display z
c0					
c1					
c2					
c3					
c4					
c5					
c6					
c7					
c8					
c9					
ca					
cb					
cc					
cd					
d0					
d1					
d2					
d3					
d4					
d5					
d6					
d7					
d8					
d9					
da					
db					
dc					
dd					
e0					
e1					
e2					
e3					
e4					
e5					
e6					
e7					
e8					
e9					
ea					
eb					
ec					
ed					
f0					
f1					
f2					
f3					
f4					
f5					
f6					
f7					
f8					
f9					
fa					
fb					
fc					
fd					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P82-Output Impedance Function, Z_{out}.

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
00	1	01			
01	1	01			
02	0	00			
03	X→	23			
04	−	34			
05	e	12			
06	2	02			
07	1	01			
08	0	00			
09	X→	23			
0a	−	34			
0b	f	15			
0c	9	11			
0d	X→	23			
10	−	34			
11	d	17			
12	9	11			
13	1	01			
14	FMT	42			
15	GoTo	44			
16	1	01			
17	6	06			
18	0	00			
19	X→	23			
1a	−	34			
1b	e	12			
1c	2	02			
1d	0	00			
20	0	00			
21	X→	23			
22	−	34			
23	f	15			
24	9	11			
25	X→	23			
26	−	34			
27	d	17			
28	9	11			
29	1	01			
2a	FMT	42			
2b	GoTo	44			
2c	9	11			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
30	FMT	42			
31	GoTo	44			
32	2	02			
33	3	03			
34	0	00			
35	X→	23			
36	−	34			
37	e	12			
38	2	02			
39	0	00			
3a	0	00			
3b	X→	23			
3c	−	34			
3d	f	15			
40	9	11			
41	X→	23			
42	−	34			
43	d	17			
44	9	11			
45	1	01			
46	FMT	42			
47	GoTo	44			
48	1	01			
49	2	02			
4a	0	00			
4b	X→	23			
4c	−	34			
4d	e	12			
50	2	02			
51	1	01			
52	0	00			
53	X→	23			
54	−	34			
55	f	15			
56	9	11			
57	X→	23			
58	−	34			
59	d	17			
5a	9	11			
5b	1	01			
5c	FMT	42			

HEWLETT·PACKARD

Step	Key	Code	Display x	Display y	Display z
60	1	01			
61	5	05			
62	0	00			
63	X→	23			
64	−	34			
65	e	12			
66	2	02			
67	2	02			
68	0	00			
69	X→	23			
6a	−	34			
6b	f	15			
6c	9	11			
6d	X→	23			
70	−	34			
71	d	17			
72	9	11			
73	1	01			
74	FMT	42			
75	GoTo	44			
76	9	11			
77	0	00			
78	FMT	42			
79	GoTo	44			
7a	2	02			
7b	3	03			
7c	0	00			
7d	X→	23			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P82-Continue.

Step	Key	Code	Display x	Display y	Display z
B 0	−	34			
1	2	12			
2	1	01			
3	9	11			
4	0	00			
5	x→	23			
6	−	34			
7	+	15			
8	9	11			
9	x→	23			
a	−	34			
b	d	17			
c	9	11			
d	1	01			
9 0	FMT	42			
1	GoTo	44			
2	FMT	42			
3	END	46			
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
8 0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage	
f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

HEWLETT·PACKARD

P83-Voltage Transfer Function, A_V.

Title P84-Trans-impedance Function, Z_{21}.

HEWLETT·PACKARD 97

Step	P83 Key	Code	Display x	Display y	Display z	Step	P84 Key	Code	Display x	Display y	Display z	Step	Key	Code	Display x	Display y	Display z
00	1	01				00	1	01				0					
01	1	01				01	5	05				1					
02	0	00				02	0	00				2					
03	X→	23				03	X→	23				3					
04	−	34				04	−	34				4					
05	R	12				05	R	12				5					
06	2	02				06	2	02				6					
07	0	00				07	0	00				7					
08	0	00				08	0	00				8					
09	X→	23				09	X→	23				9					
0a	−	34				0a	−	34				a					
0b	f	15				0b	f	15				b					
0c	9	11				0c	9	11				c					
0d	X→	23				0d	X→	23				d					

HEWLETT·PACKARD 98

Step	P83 Key	Code	Display x	Display y	Display z	Step	P84 Key	Code	Display x	Display y	Display z	Step	Key	Code	Display x	Display y	Display z
10	−	34				10	−	34				0					
11	d	17				11	d	17				1					
12	9	11				12	9	11				2					
13	1	01				13	1	01				3					
14	FMT	42				14	FMT	42				4					
15	GoTo	44				15	GoTo	44				5					
16	1	01				16	1	01				6					
17	2	02				17	6	06				7					
18	0	00				18	0	00				8					
19	X→	23				19	X→	23				9					
1a	−	34				1a	−	34				a					
1b	R	12				1b	R	12				b					
1c	1	01				1c	1	01				c					
1d	9	11				1d	9	11				d					

HEWLETT·PACKARD 99

Step	P83 Key	Code	Display x	Display y	Display z	Step	P84 Key	Code	Display x	Display y	Display z	Step	Key	Code	Display x	Display y	Display z
20	0	00				20	0	00									
21	X→	23				21	X→	23									
22	−	34				22	−	34									
23	f	15				23	f	15									
24	9	11				24	9	11									
25	X→	23				25	X→	23									
26	−	34				26	−	34									
27	d	17				27	d	17									
28	9	11				28	9	11									
29	1	01				29	1	01									
2a	FMT	42				2a	FMT	42									
2b	GoTo	44				2b	GoTo	44									
2c	FMT	42				2c	FMT	42									
2d	END	46				2d	END	46									

HEWLETT·PACKARD 67

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P2-Response Time Function Computation Initialization.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	1	02			
02	4	04			
03	6	06			
04	FMT	42			
05	y→	40			
06	2	02			
07	2	02			
08	9	11			
09	↑	27			
0a	2	02			
0b	1	01			
0c	0	00			
0d	arc+	60			
10	0	00			
11	↑	27			
12	f	15			
13	FMT	42			
14	y→	40			
15	RCL	60			
16	x↔y	50			
17	2	02			
18	1	01			
19	0	00			
1a	↑	27			
1b	1	01			
1c	GoTo	44			
1d	0	00			
20	d	17			
21	1	01			
22	0	00			
23	FMT	42			
24	GoTo	44			
25	3	03			
26	FMT	42			
27	GoTo	44			
28	1	01			
29	1	01			
2a	FMT	42			
2b	GoTo	44			
2c	2	02			
2d	4	04			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	5	05			
31	FMT	42			
32	π	56			
33	1	27			
34	2	02			
35	4	04			
36	6	06			
37	FMT	42			
38	π	56			
39	x↔y	50			
3a	4	04			
3b	6	14			
3c	1	01			
3d	↑	27			
40	2	02			
41	4	04			
42	6	06			
43	FMT	42			
44	+	33			
45	8	10			
46	FMT	42			
47	GoTo	44			
48	GoTo	44			
49	2	02			
4a	1	01			
4b	0	00			
4c	↑	27			
4d	2	02			
50	4	04			
51	6	06			
52	FMT	42			
53	π	56			
54	↑	27			
55	2	02			
56	4	04			
57	7	07			
58	FMT	42			
59	π	56			
5a	X	36			
5b	0	00			
5c	PRNT	45			
5d	Clear	20			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60	2	02			
61	1	01			
62	0	00			
63	↑	27			
64	2	02			
65	2	02			
66	9	11			
67	arc+	60			
68	0	00			
69	↑	27			
6a	e	12			
6b	↑	27			
6c	FMT	42			
6d	π	56			
70	PRNT	45			
71	RCL	61			
72	x↔y	50			
73	7	07			
74	6	14			
75	1	01			
76	↑	27			
77	0	00			
78	GoTo	44			
79	6	06			
7a	7	07			
7b	END	46			
7c					
7d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P3-Final Calculation Of Response Time Function, r(t).

HEWLETT-PACKARD 25

Step	Key	Code	Display x	Display y	Display z
0 0	2	02			
1	4	04			
2	4	04			
3	FMT	42			
4	π	56			
5	↑	27			
6	2	02			
7	4	04			
8	2	02			
9	FMT	42			
a	y→	40			
b	1	01			
c	9	11			
d	0	00			
1 0	↑	27			
1	2	02			
2	3	03			
3	1	01			
4	FMT	42			
5	y→	40			
6	4	04			
7	FMT	42			
8	GoTo	44			
9	2	02			
a	3	03			
b	6	06			
c	FMT	42			
d	π	56			
2 0	↑	27			
1	2	02			
2	1	01			
3	9	11			
4	FMT	42			
5	π	56			
6	X	36			
7	2	02			
8	3	03			
9	0	00			
a	FMT	42			
b	y→	40			
c	7	07			
d	FMT	42			

HEWLETT-PACKARD 22

Step	Key	Code	Display x	Display y	Display z
3 0	GoTo	44			
1	2	02			
2	3	03			
3	4	04			
4	FMT	42			
5	π	56			
6	↑	27			
7	2	02			
8	3	03			
9	0	00			
a	FMT	42			
b	+	33			
c	2	02			
d	4	04			
4 0	3	03			
1	FMT	42			
2	π	56			
3	↑	27			
4	2	02			
5	4	04			
6	2	02			
7	FMT	42			
8	y→	40			
9	2	02			
a	0	00			
b	0	00			
c	↑	27			
d	2	02			
5 0	3	03			
1	1	01			
2	FMT	42			
3	y→	40			
4	4	04			
5	FMT	42			
6	GoTo	44			
7	7	07			
8	FMT	42			
9	GoTo	44			
a	2	02			
b	3	03			
c	4	04			
d	FMT	42			

Step	Key	Code	Display x	Display y	Display z
6 0	π	56			
1	↑	27			
2	2	02			
3	3	03			
4	0	00			
5	FMT	42			
6	−	34			
7	2	02			
8	3	03			
9	0	00			
a	FMT	42			
b	π	56			
c	↑	27			
d	2	02			
7 0	3	03			
1	6	06			
2	FMT	42			
3	π	56			
4	÷	35			
5	2	02			
6	2	02			
7	9	11			
8	FMT	42			
9	y→	40			
a	FMT	42			
b	END	46			
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P4-Calculation of $\Sigma \frac{1}{x}$ For Use In P3.

HEWLETT·PACKARD 65

Step	Key	Code	Display x	Display y	Display z
0 0	Clear	20			
1	f	15			
2	↑	27			
3	2	02			
4	3	03			
5	1	01			
6	FMT	42			
7	π	56			
8	+	33			
9	↓	25			
a	FMT	42			
b	π	56			
c	↑	27			
d	2	02			
1 0	4	04			
1	7	07			
2	FMT	42			
3	π	56			
4	ln X	65			
5	↑	27			
6	f	15			
7	X	36			
8	↓	25			
9	e^x	74			
a	÷	35			
b	0	00			
c	acc+	60			
d	2	02			
2 0	4	04			
1	2	02			
2	FMT	42			
3	π	56			
4	↑	27			
5	f	15			
6	$x^{\frac{1}{y}}$	50			
7	3	03			
8	2	02			
9	0	00			
a	$X_{<y}$	30			
b	1	01			
c	acc+	60			
d	GoTo	44			

HEWLETT·PACKARD 65

Step	Key	Code	Display x	Display y	Display z
3 0	0	00			
1	1	01			
2	.	12			
3	↑	27			
4	2	02			
5	3	03			
6	6	06			
7	FMT	42			
8	y→	40			
9	FMT	42			
a	END	46			
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

HEWLETT·PACKARD 65

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P5-Calculation of $\sum_{i=1}^{n} \frac{q(k-x-y)}{(n-j)!j!}$ For Use In P3.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	1	01			
01	↑	27			
02	2	02			
03	4	04			
04	.0	00			
05	FMT	42			
06	y→	40			
07	Clear	20			
08	2	02			
09	3	03			
0a	3	03			
0b	FMT	42			
0c	y→	40			
0d	2	02			
10	4	04			
11	0	00			
12	FMT	42			
13	π	56			
14	↑	27			
15	2	02			
16	3	03			
17	9	11			
18	FMT	42			
19	y→	40			
1a	6	06			
1b	FMT	42			
1c	GoTo	44			
1d	2	02			
20	3	03			
21	9	11			
22	FMT	42			
23	π	56			
24	↑	27			
25	2	02			
26	3	03			
27	2	02			
28	FMT	42			
29	y→	40			
2a	2	02			
2b	4	04			
2c	1	01			
2d	FMT	42			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	π	56			
31	↑	27			
32	2	02			
33	4	04			
34	0	00			
35	FMT	42			
36	π	56			
37	−	34			
38	2	02			
39	3	03			
3a	9	11			
3b	FMT	42			
3c	y→	40			
3d	6	06			
40	FMT	42			
41	GoTo	44			
42	2	02			
43	3	03			
44	9	11			
45	FMT	42			
46	π	56			
47	↑	27			
48	2	02			
49	3	03			
4a	2	02			
4b	FMT	42			
4c	X	36			
4d	2	02			
50	3	03			
51	1	01			
52	FMT	42			
53	π	56			
54	↑	27			
55	2	02			
56	4	04			
57	0	00			
58	FMT	42			
59	π	56			
5a	−	34			
5b	↓	25			
5c	FMT	42			
5d	π	56			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60	↑	27			
61	2	02			
62	3	03			
63	2	02			
64	FMT	42			
65	π	56			
66	÷	35			
67	2	02			
68	4	04			
69	0	00			
6a	FMT	42			
6b	π	56			
6c	↑	27			
6d	2	02			
70	÷	35			
71	↓	25			
72	INTX	64			
73	↑	27			
74	2	02			
75	X	36			
76	2	02			
77	4	04			
78	0	00			
79	FMT	42			
7a	π	56			
7b	x≥y	50			
7c	8	10			
7d	9	11			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title #5-Continue.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
8 0	↓	25			
1	2	02			
2	3	03			
3	3	03			
4	FMT	42			
5	-	34			
6	Go To	44			
7	9	11			
8	1	01			
9	↓	25			
a	2	02			
b	3	03			
c	3	03			
d	FMT	42			
9 0	+	33			
1	2	02			
2	4	04			
3	1	01			
4	FMT	42			
5	π	56			
6	↑	27			
7	2	02			
8	4	04			
9	0	00			
a	FMT	42			
b	π	56			
c	x≷y	50			
d	0	13			
A 0	↓	25			
1	1	01			
2	↑	27			
3	2	02			
4	4	04			
5	0	00			
6	FMT	42			
7	+	33			
8	Go To	44			
9	0	00			
a	d	17			
b	FMT	42			
c	END	43			
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P6-Sub-routine To Evaluate Factorial X, X!

HEWLETT-PACKARD 67

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	3	03			
03	9	11			
04	FMT	42			
05	π	56			
06	x≷y	50			
07	2	02			
08	a	13			
09	x→	23			
0a	d	17			
0b	1	01			
0c	x≷y	30			
0d	acc+	60			

HEWLETT-PACKARD 67

Step	Key	Code	Display x	Display y	Display z
10	e	12			
11	lnx	65			
12	↑	27			
13	0	00			
14	x≷y	30			
15	acc+	60			
16	d	17			
17	↑	27			
18	e	12			
19	x≷y	50			
1a	2	02			
1b	4	04			
1c	1	01			
1d	↑	27			

HEWLETT-PACKARD 67

Step	Key	Code	Display x	Display y	Display z
20	0	00			
21	GoTo	44			
22	0	00			
23	d	17			
24	RCL	61			
25	e^x	74			
26	↑	27			
27	GoTo	44			
28	2	02			
29	c	16			
2a	1	01			
2b	↑	27			
2c	2	02			
2d	3	03			

HEWLETT-PACKARD 67

Step	Key	Code	Display x	Display y	Display z
30	9	11			
31	FMT	42			
32	y→	40			
33	FMT	42			
34	END	46			
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

HEWLETT-PACKARD 67

Step	Key	Code	Display x	Display y	Display z
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					

HEWLETT-PACKARD 67

Step	Key	Code	Display x	Display y	Display z
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
5a					
5b					
5c					
5d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P7-Computation Of $\sum_{n=1}^{N} \frac{a_n n!}{T^n} \cdot \sum_{j=1}^{n} \frac{e^{(j-1)T(-1)^j}}{(n-j)!\, j!}$ For Use In r(t) Analysis.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	3	03			
03	4	04			
04	FMT	42			
05	y→	40			
06	1	01			
07	↑	27			
08	2	02			
09	4	04			
0a	1	01			
0b	FMT	42			
0c	y→	40			
0d	2	02			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
10	9	11			
11	↑	27			
12	2	02			
13	3	03			
14	1	01			
15	FMT	42			
16	+	33			
17	5	05			
18	FMT	42			
19	GoTo	44			
1a	2	02			
1b	3	03			
1c	1	01			
1d	FMT	42			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
20	π	56			
21	↑	27			
22	2	02			
23	9	11			
24	−	34			
25	2	02			
26	4	04			
27	1	01			
28	FMT	42			
29	π	56			
2a	+	33			
2b	↓	25			
2c	FMT	42			
2d	π	56			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
30	↑	27			
31	2	02			
32	3	03			
33	3	03			
34	FMT	42			
35	X	36			
36	2	02			
37	4	04			
38	7	07			
39	FMT	42			
3a	π	56			
3b	$\ln x$	65			
3c	↑	27			
3d	2	02			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
40	4	04			
41	1	01			
42	FMT	42			
43	π	56			
44	X	36			
45	↓	25			
46	e^x	74			
47	↑	27			
48	2	02			
49	3	03			
4a	3	03			
4b	FMT	42			
4c	÷	35			
4d	2	02			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
50	4	04			
51	1	01			
52	FMT	42			
53	π	56			
54	↑	27			
55	2	02			
56	3	03			
57	9	11			
58	FMT	42			
59	y→	40			
5a	6	06			
5b	FMT	42			
5c	GoTo	44			
5d	2	02			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
60	3	03			
61	9	11			
62	FMT	42			
63	π	56			
64	↑	27			
65	2	02			
66	3	03			
67	3	03			
68	FMT	42			
69	X	36			
6a	2	02			
6b	3	03			
6c	3	03			
6d	FMT	42			

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
70	π	56			
71	↑	27			
72	2	02			
73	3	03			
74	4	04			
75	FMT	42			
76	+	33			
77	2	02			
78	4	04			
79	2	02			
7a	FMT	42			
7b	π	56			
7c	↑	27			
7d	2	02			

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P7-Continue.

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
80	4	04			
81	1	01			
82	FIX	42			
83	π	56			
84	x↔y	50			
85	9	11			
86	3	03			
87	1	01			
88	x↔y	30			
89	2	02			
8a	4	04			
8b	1	01			
8c	FIX	42			
8d	+	33			
90	GTO	44			
91	1	01			
92	7	07			
93	FIX	42			
94	END	46			
95					
96					
97					
98					
99					
9a					
9b					
9c					
9d					
a0					
a1					
a2					
a3					
a4					
a5					
a6					
a7					
a8					
a9					
aa					
ab					
ac					
ad					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
b0					
b1					
b2					
b3					
b4					
b5					
b6					
b7					
b8					
b9					
ba					
bb					
bc					
bd					
c0					
c1					
c2					
c3					
c4					
c5					
c6					
c7					
c8					
c9					
ca					
cb					
cc					
cd					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
d0					
d1					
d2					
d3					
d4					
d5					
d6					
d7					
d8					
d9					
da					
db					
dc					
dd					
e0					
e1					
e2					
e3					
e4					
e5					
e6					
e7					
e8					
e9					
ea					
eb					
ec					
ed					

HEWLETT-PACKARD

Step	Key	Code	Display x	Display y	Display z
f0					
f1					
f2					
f3					
f4					
f5					
f6					
f7					
f8					
f9					
fa					
fb					
fc					
fd					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P8-Time Shift Program: e(K-1)T = e(KT), and r(K-1)T = r(KT).

HEWLETT·PACKARD 42

Step	Key	Code	Display x	Display y	Display z
00	Clear	20			
01	2	02			
02	1	01			
03	1	01			
04	↑	27			
05	2	02			
06	1	01			
07	0	00			
08	acc+	60			
09	e	12			
0a	FIX	42			
0b	π	56			
0c	↑	27			
0d	f	15			

HEWLETT·PACKARD 42

Step	Key	Code	Display x	Display y	Display z
10	FIX	42			
11	y→	40			
12	e	12			
13	↑	27			
14	1	01			
15	0	00			
16	+	33			
17	↓	25			
18	FIX	42			
19	π	56			
1a	↑	27			
1b	f	15			
1c	↑	27			
1d	1	01			

HEWLETT·PACKARD 42

Step	Key	Code	Display x	Display y	Display z
20	0	00			
21	+	33			
22	↓	25			
23	FIX	42			
24	y→	40			
25	2	02			
26	1	01			
27	9	11			
28	↑	27			
29	e	12			
2a	x≷y	50			
2b	3	03			
2c	+	04			
2d	1	01			

HEWLETT·PACKARD 42

Step	Key	Code	Display x	Display y	Display z
30	↑	27			
31	GoTo	44			
32	0	00			
33	8	10			
34	FIX	42			
35	END	46			
36					
37					
38					
39					
3a					
3b					
3c					
3d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1a					
1b					
1c					
1d					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					
2a					
2b					
2c					
2d					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

Step	Key	Code	Display x	Display y	Display z
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0a					
0b					
0c					
0d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P10-Sample Excitation Function, U(KT) = 1 For K≥0.

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
00	2	02			
01	4	04			
02	6	06			
03	FMT	42			
04	π	56			
05	↑	27			
06	2	02			
07	4	04			
08	7	07			
09	FMT	42			
0a	π	56			
0b	X	36			
0c	1	01			
0d	Exp	26			

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
10	CHS	32			
11	5	05			
12	0	00			
13	x≷y	53			
14	2	02			
15	2	02			
16	1	01			
17	↑	27			
18	2	02			
19	1	01			
1a	9	11			
1b	FMT	42			
1c	y→	40			
1d	GoTo	44			

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
20	2	02			
21	9	11			
22	0	00			
23	↑	27			
24	2	02			
25	1	01			
26	9	11			
27	FMT	42			
28	y→	40			
29	FMT	42			
2a	END	46			
2b					
2c					
2d					

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
3a					
3b					
3c					
3d					

HEWLETT-PACKARD 97

Step	Key	Code	Display x	Display y	Display z
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
4a					
4b					
4c					
4d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

Title P11-Output Sub-routine For The Plot of Response VS Time.

HEWLETT·PACKARD 42

Step	Key	Code	Display x	Display y	Display z
0 0	2	02			
1	2	02			
2	9	11			
3	FMT	42			
4	π	56			
5	↑	27			
6	1	01			
7	0	00			
8	8	10			
9	FMT	42			
a	π	56			
b	X→	27			
c	a	13			
d	−	34			
1 0	1	01			
1	0	00			
2	9	11			
3	FMT	42			
4	π	56			
5	X→	23			
6	b	14			
7	÷	35			
8	5	05			
9	0	00			
a	0	00			
b	X	36			
c	2	02			
d	↓	04			
2 0	6	06			
1	FMT	42			
2	π	56			
3	↑	27			
4	2	02			
5	↓	04			
6	7	07			
7	FMT	42			
8	π	56			
9	X	36			
a	1	01			
b	0	00			
c	6	06			
d	FMT	42			

HEWLETT·PACKARD 42

Step	Key	Code	Display x	Display y	Display z
3 0	π	56			
1	−	34			
2	1	01			
3	0	00			
4	7	07			
5	FMT	42			
6	π	56			
7	÷	35			
8	5	05			
9	0	00			
a	0	00			
b	X	36			
c	↓	25			
d	FMT	42			
4 0	↓	25			
1	FMT	42			
2	↑	27			
3	↑	27			
4	2	02			
5	↓	01			
6	9	11			
7	FMT	42			
8	π	56			
9	↑	27			
a	a	13			
b	−	94			
c	b	14			
d	÷	35			
5 0	5	05			
1	0	00			
2	0	00			
3	X	36			
4	↓	25			
5	X↔Y	30			
6	FMT	42			
7	↓	25			
8	FMT	42			
9	↑	27			
a	FMT	42			
b	END	46			
c					
d					

HEWLETT·PACKARD 42

Step	Key	Code	Display x	Display y	Display z
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
a					
b					
c					
d					

Storage

f	
e	
d	
c	
b	
a	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

APPENDIX III

OPERATION PROCEDURES FOR THE S-PARAMETERS INPUT OPTION

Special sub-programs are devised to accept thr scattering parameters of a circuit block as valid input data, but still maintain swept frequency analysis capability.

The swept frequency analysis capability is based on the generation of the S-parameters at any frequency f_i by interpolation of two sets of S-parameters at two given frequencies. An "S - A" sub-routine converts the S-parameters into the regular chain matrix for use in the regular analysis procedures by the circuit analysis program (Frequency domain) P1.

Outlined below are the operation procedures of this input option.

The operation begins by entering the circuit block information codes corresponding to the S-parameters entry option:

P = 3 (code for cascaded circuit block)
Q = 3 (S-parameter input option code when P = 3)

Input data of the S-parameters are accepted via sub-program P7 which takes 2 sets of S-parameters at 2 given frequencies.

Sub-programs P92 - P94 are responsible for the

conversion of S-parameters to chain matrix, while P95 provides interpolation computation. The overall operation is initiated by P33 which ensures the loading of the resulting chain matrix into matrix B.

Following are the operation sequence of this option:

. Program loading:

Load P7, 33, 92, 93, 94, 95 in the manner shown in section 3.2 for typical circuit blocks.

. Program execution:

The following data is entered in the Input data sub-program (P0) to describe circuit block #i is defined by S-parameters.

Step	User action	Display X	Y	Z
		i	i	i
1	Enter: 3 into X- and Y- registers.	3	3	
2	Press: CONTINUE.	1	33	i
3	Enter: f_a into X-register.	f_a		
4	Press: CONTINUE.	2	33	i
5	Enter: f_b into X-register.	f_b		
6	Press: CONTINUE.	3	33	i
7	Enter: Characteristic impedance of system, Z_o, into X-register.	Z_o		
8	Press: CONTINUE. Proceed with the entry of other circuit block.	i+1	i+1	i+1

At the conclusion of P0 when display

X	Y	Z
1	6	6

is seen, enter 7 into X-register, and press CONTINUE.

Step	User action	Display X	Y	Z
		1	1	1
1	Enter: S_{11} of circuit block at frequency f_a. Magnitude into X-register, angle in degrees into Y-register.	S_{11}	Θ_{11}	
2	Press: CONTINUE.	2	1	1
3	Enter: S_{12}.	S_{12}	Θ_{12}	
4	Press: CONTINUE.	1	2	1
5	Enter: S_{21}.	S_{21}	Θ_{21}	
6	Press: CONTINUE.	2	2	1
7	Enter: S_{22}.	S_{22}	Θ_{22}	
8	Press: CONTINUE.	1	1	2
.	(Steps 1 - 7 are repeated for data at f_b)			
.				
.				
9	When see display	1	6	6
10	Enter: 6 into X-register (if alteration is needed, and Step 25 a-f of section 3.3 follows) (If no alteration is needed, go to Step 11)			
11	Press: CONTINUE.			

Circuit analysis program (P1) will be automatically activated for circuit analysis.

APPENDIX IV

A SAMPLE OF THE EXTENDED MEMORY MAP, RECORDING FORM

HEWLETT-PACKARD

Title _____ Date _____ Page _____ of _____

Name _____

9101A MEMORY MAP

0		50		100		150	200
1		51		101		151	201
2		52		102		152	202
3		53		103		153	203
4		54		104		154	204
5		55		105		155	205
6		56		106		156	206
7		57		107		157	207
8		58		108		158	208
9		59		109		159	209
10		60		110		160	210
11		61		111		161	211
12		62		112		162	212
13		63		113		163	213
14		64		114		164	214
15		65		115		165	215
16		66		116		166	216
17		67		117		167	217
18		68		118		168	218
19		69		119		169	219
20		70		120		170	220
21		71		121		171	221
22		72		122		172	222
23		73		123		173	223
24		74		124		174	224
25		75		125		175	225
26		76		126		176	226
27		77		127		177	227
28		78		128		178	228
29		79		129		179	229
30		80		130		180	230
31		81		131		181	231
32		82		132		182	232
33		83		133		183	233
34		84		134		184	234
35		85		135		185	235
36		86		136		186	236
37		87		137		187	237
38		88		138		188	238
39		89		139		189	239
40		90		140		190	240
41		91		141		191	241
42		92		142		192	242
43		93		143		193	243
44		94		144		194	244
45		95		145		195	245
46		96		146		196	246
47		97		147		197	247
48		98		148		198	
49		99		149		199	

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